

Compal Confidential

JAWD0 Schematics Document

AMD Griffin Processor with RS780M+SB700

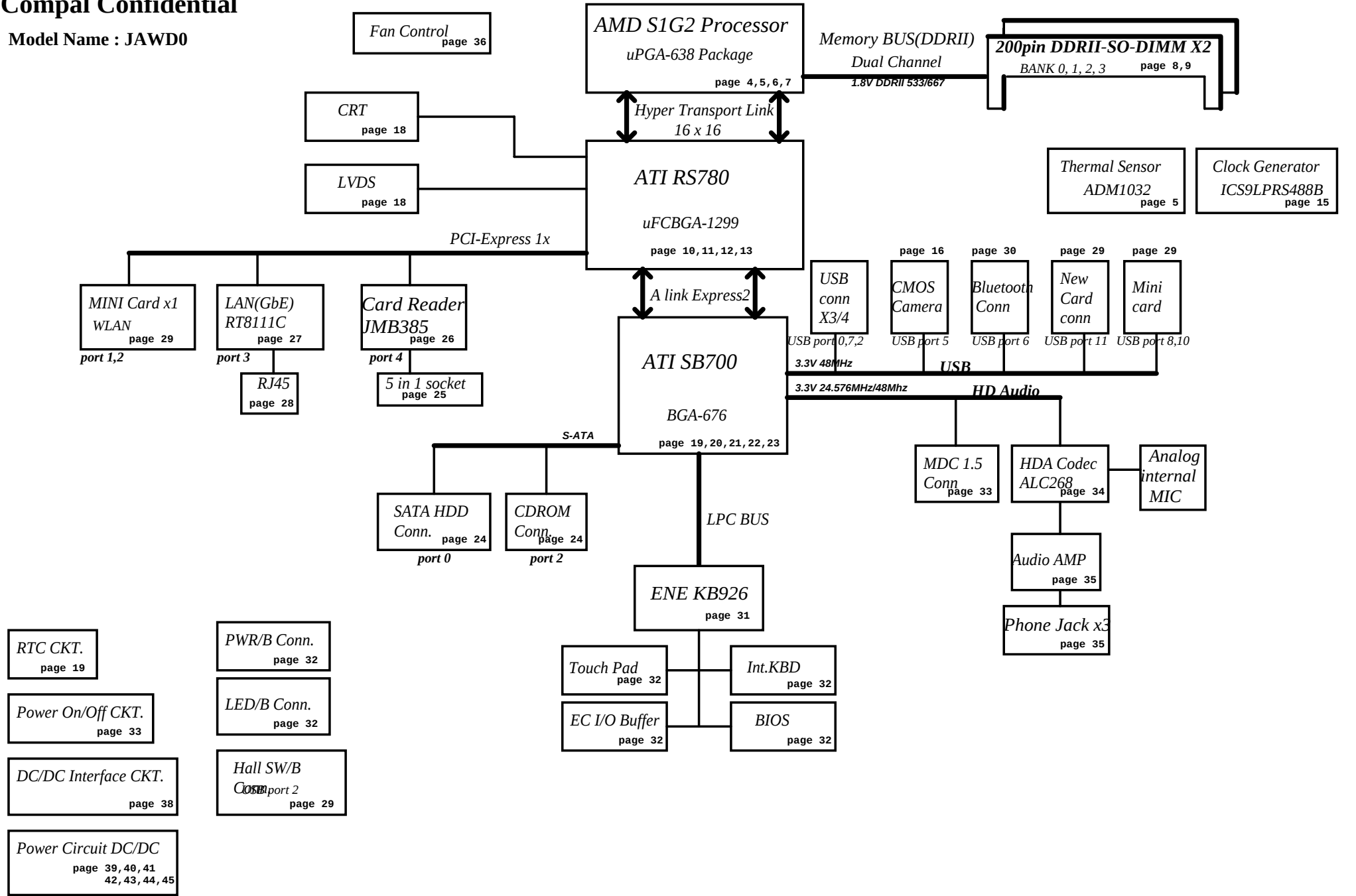
2008-07-01

REV:1.0

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				Date: Tuesday, August 19, 2008	

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Model Name : JAWD0



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		

EC SM Bus2 address

SB700 SM Bus 0 address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
Minicard	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

BOARD ID Table

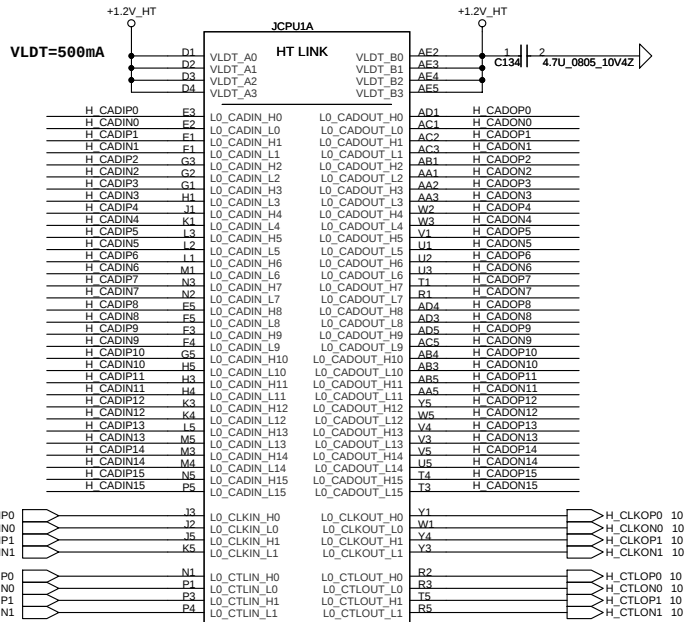
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure

PROJECT ID Table

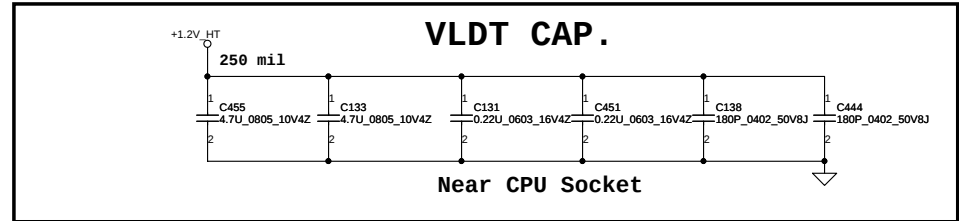
Board ID	PROJECT
0	JALB0
1	
2	
3	
4	
5	JAWD0
6	
7	JALC0



6090022100G_B

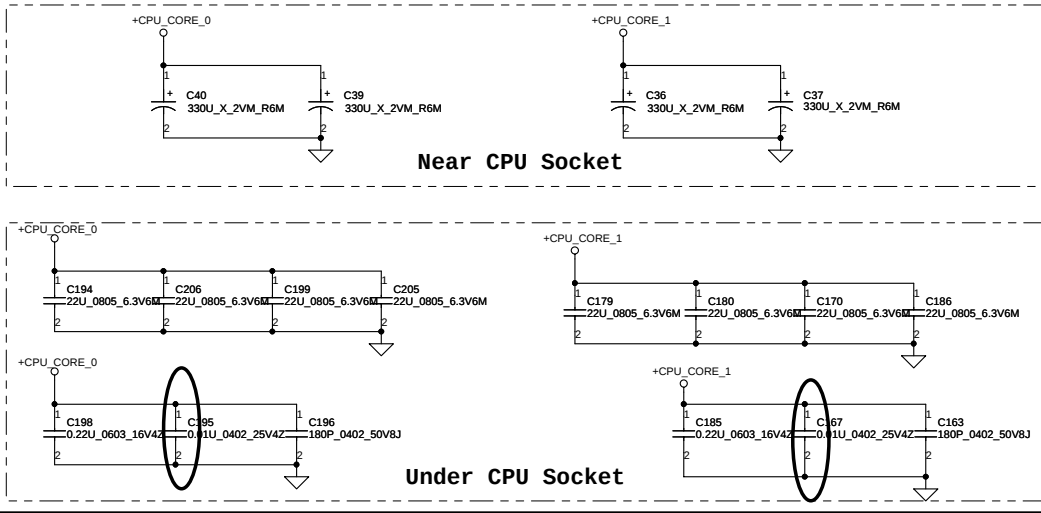
Athlon 64 S1

Processor Socket

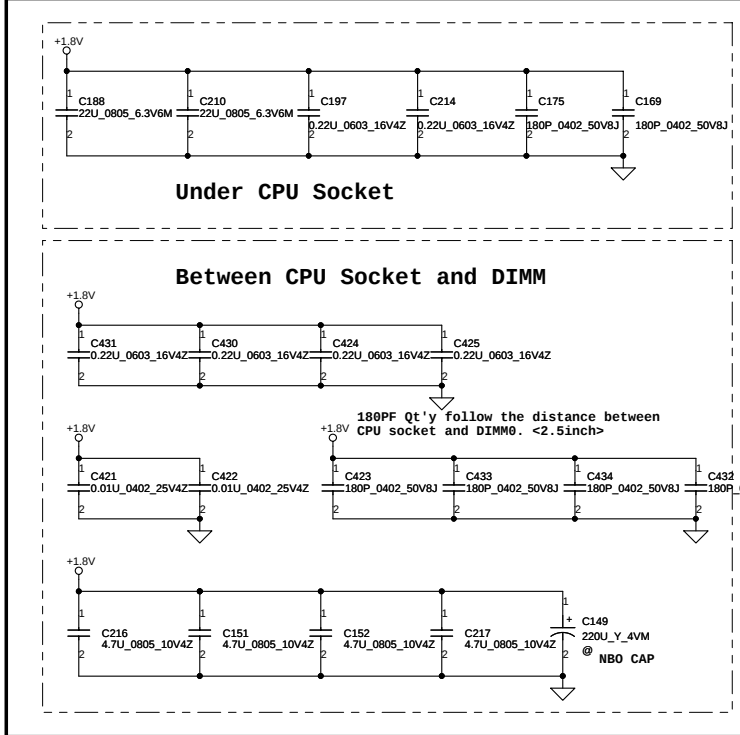


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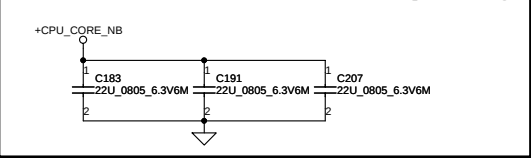
VDD(+CPU_CORE) decoupling.



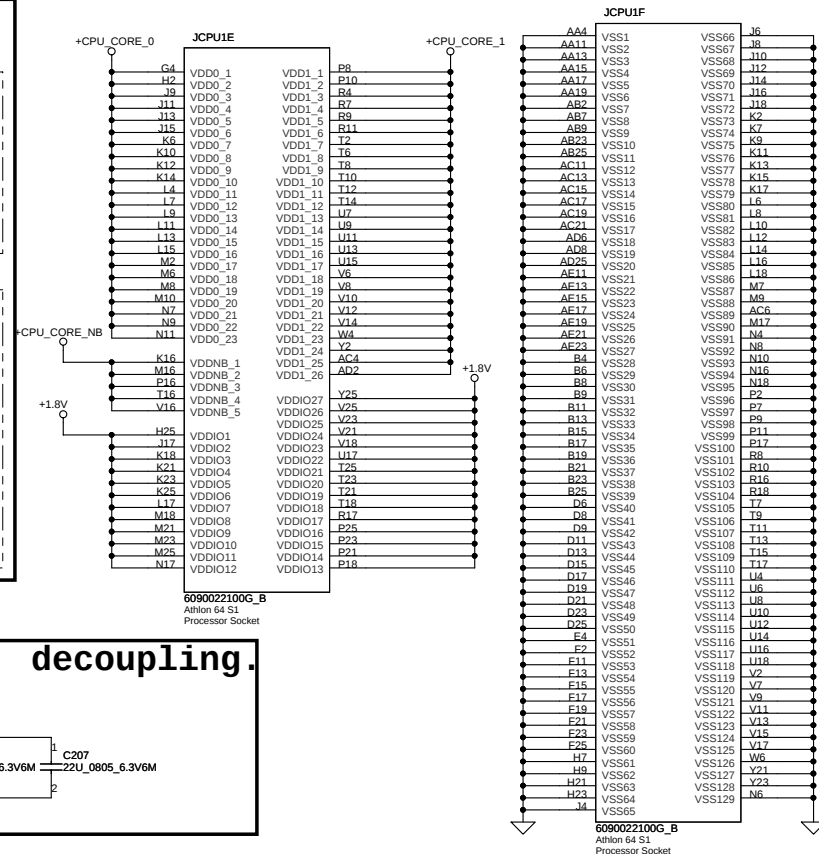
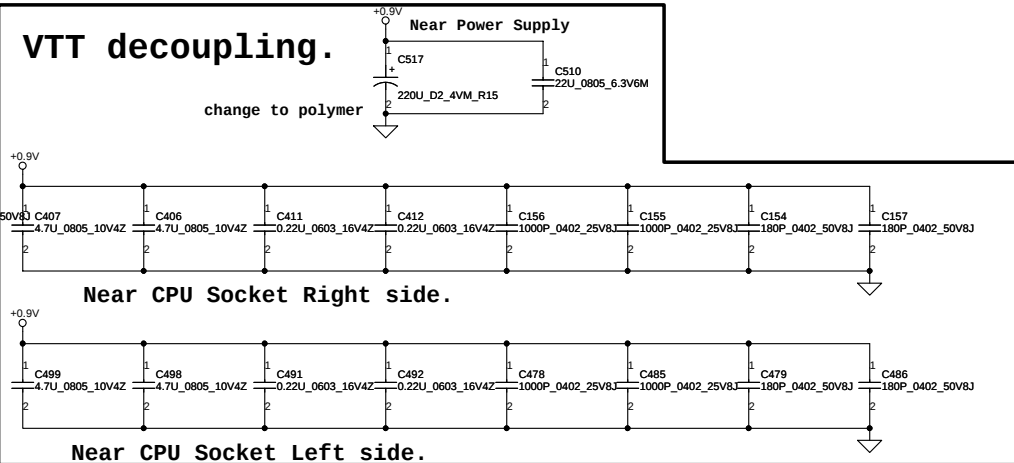
VDDIO decoupling.



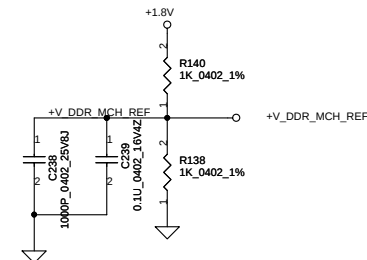
+CPU_CORE_NB decoupling.



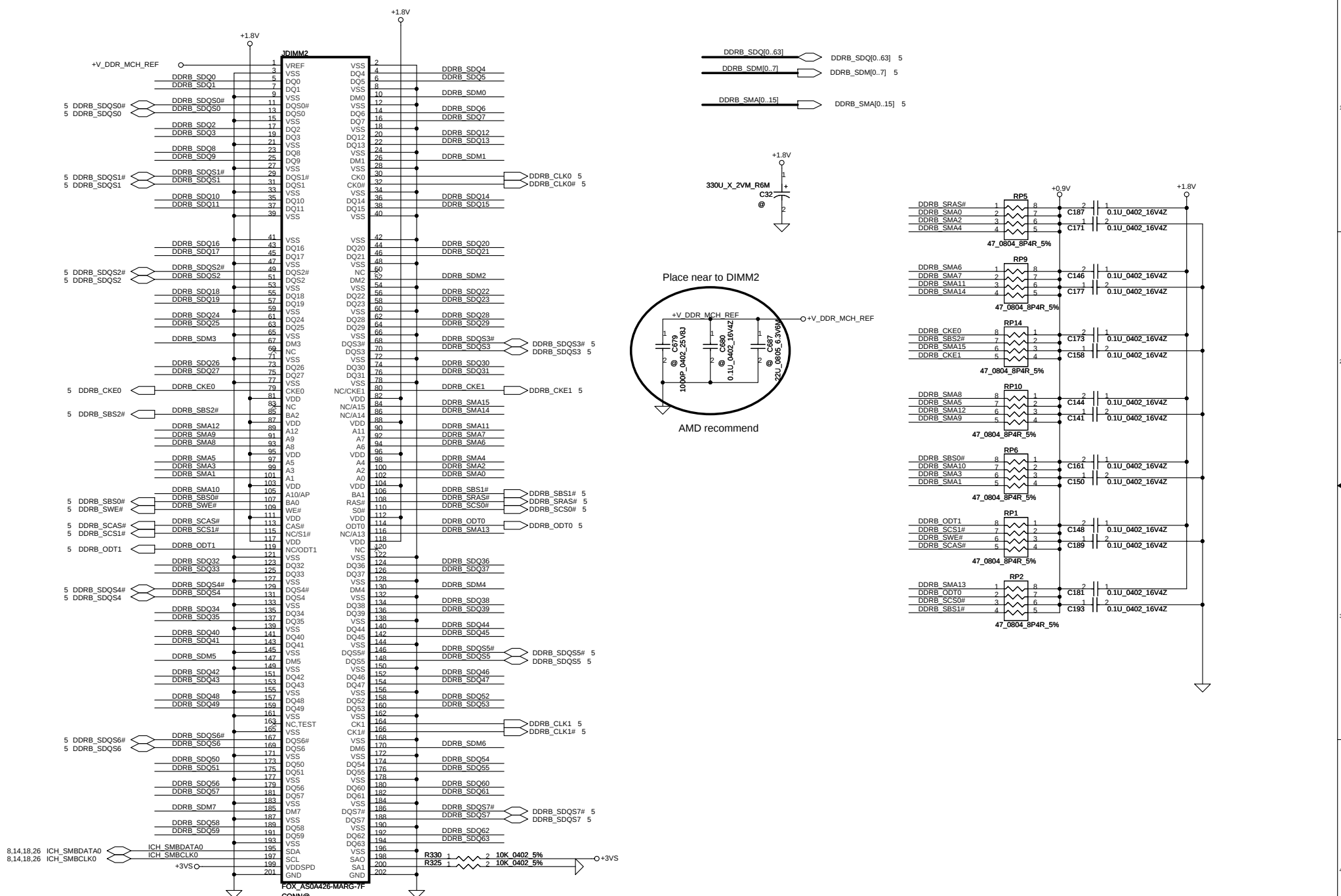
VTT decoupling.



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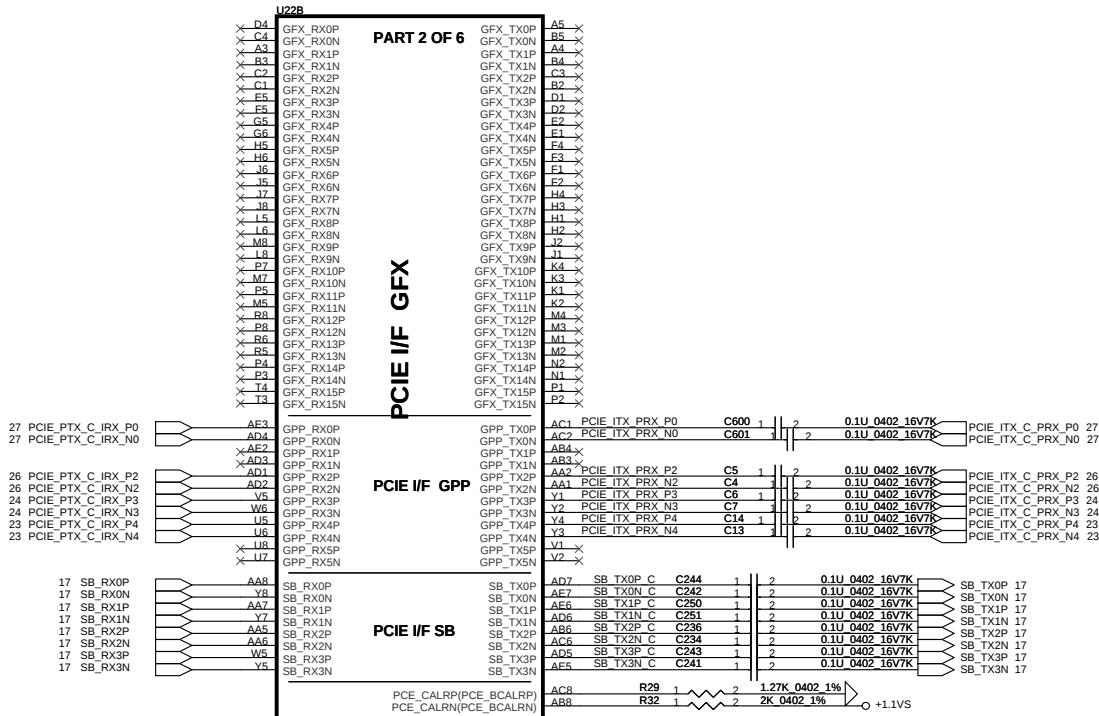


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DIMM1 REV H:9.2mm (BOT)

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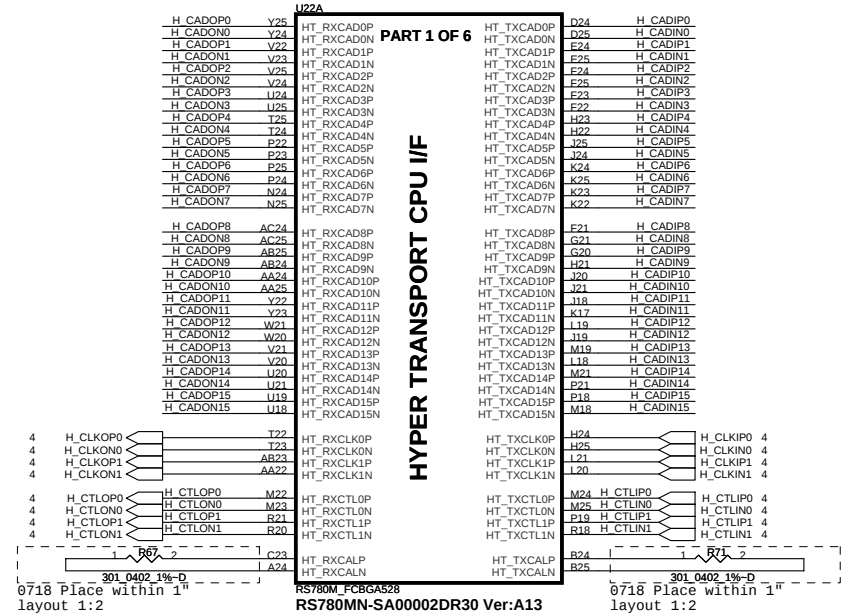
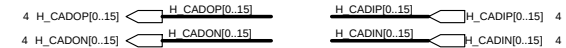


New Card

Mini1

GLAN

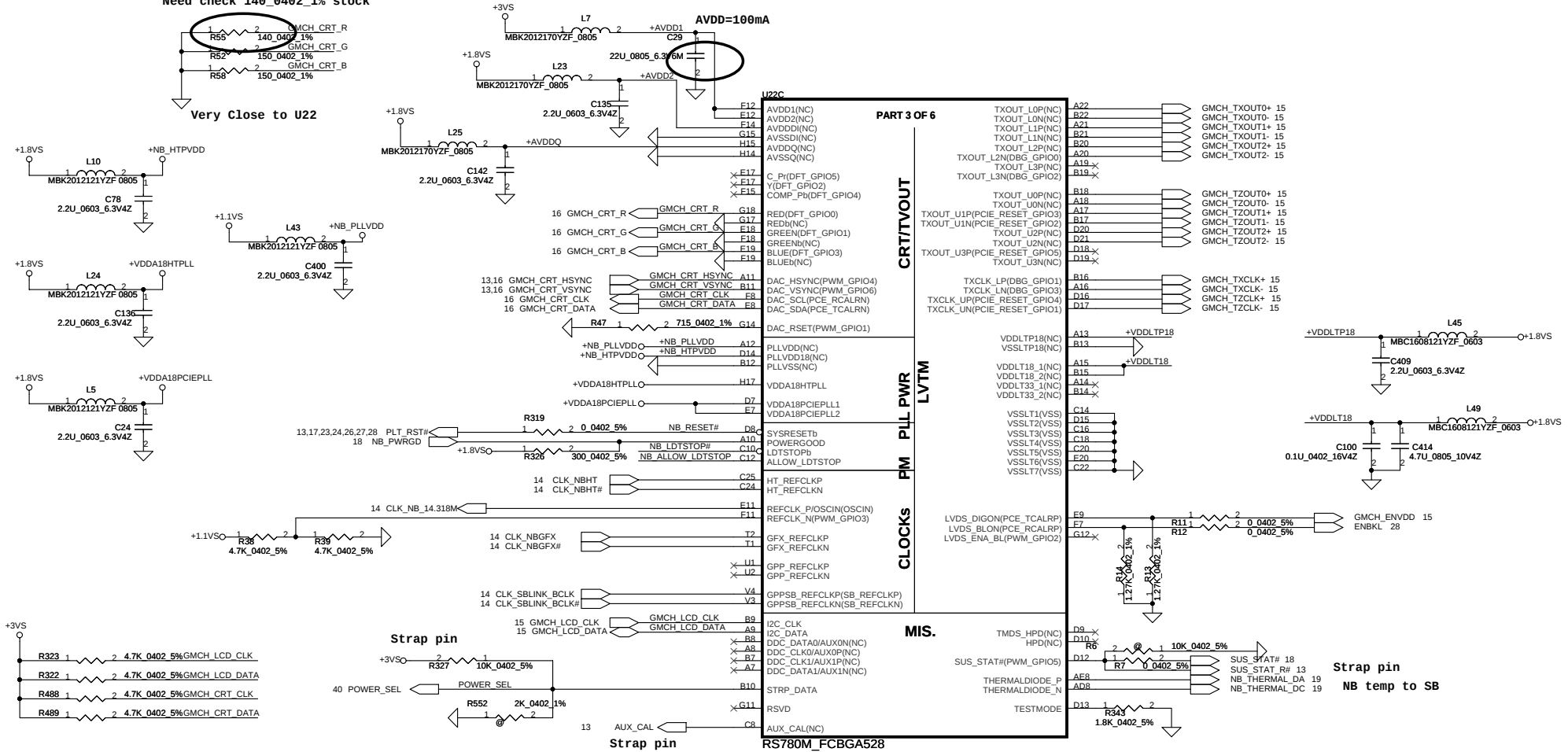
Card Reader



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Need check 140_0402_1% stock

Very Close to U22



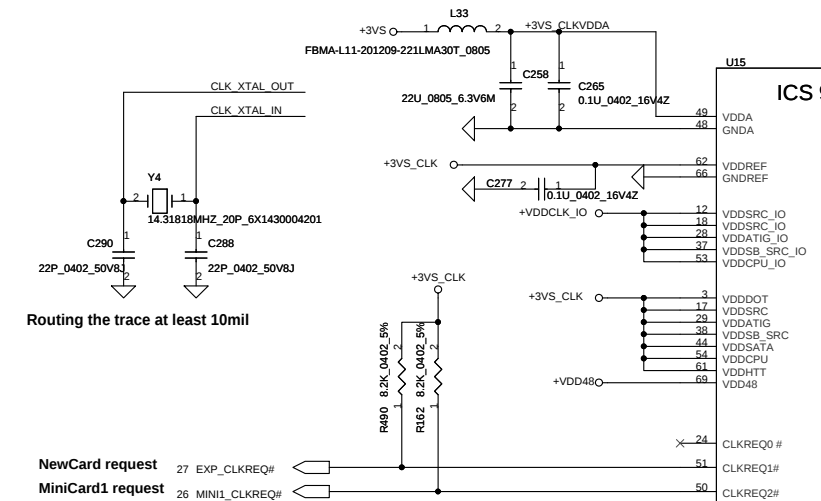
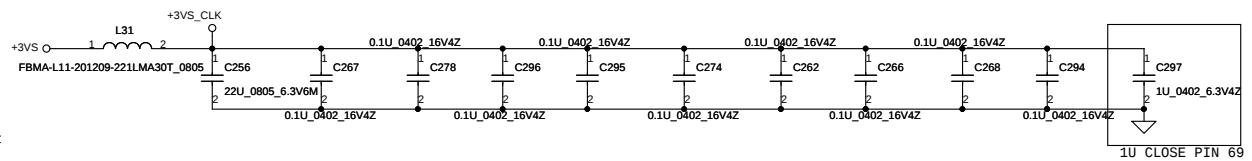
Strap pin

Strap pin
NB temp to SB

Strap pin

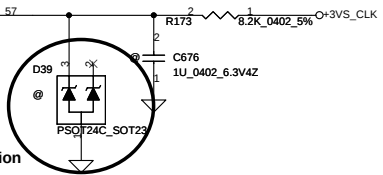
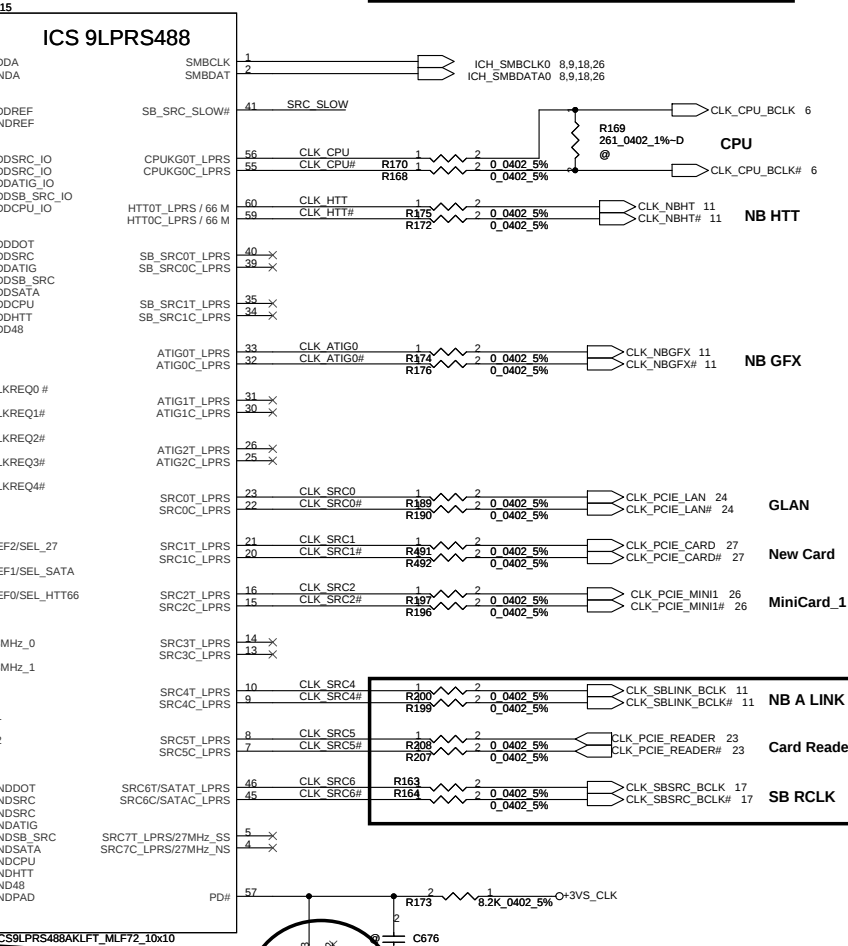
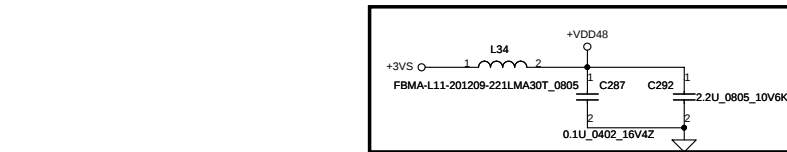
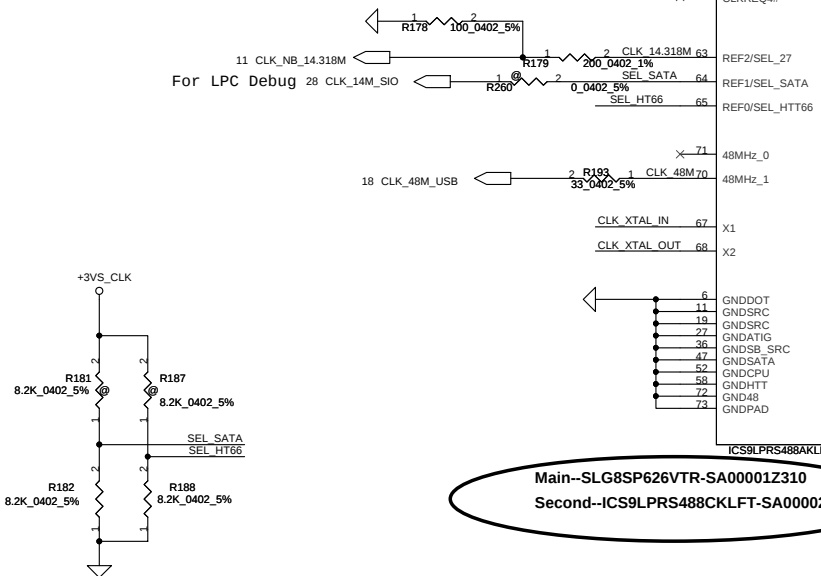
RS780M-FCBGA528
RS780MN-SA00002DR30 Ver:A13

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Routing the trace at least 10mil

NewCard request	27	EXP_CLKREQ#
MiniCard1 request	26	MINI1_CLKREQ#



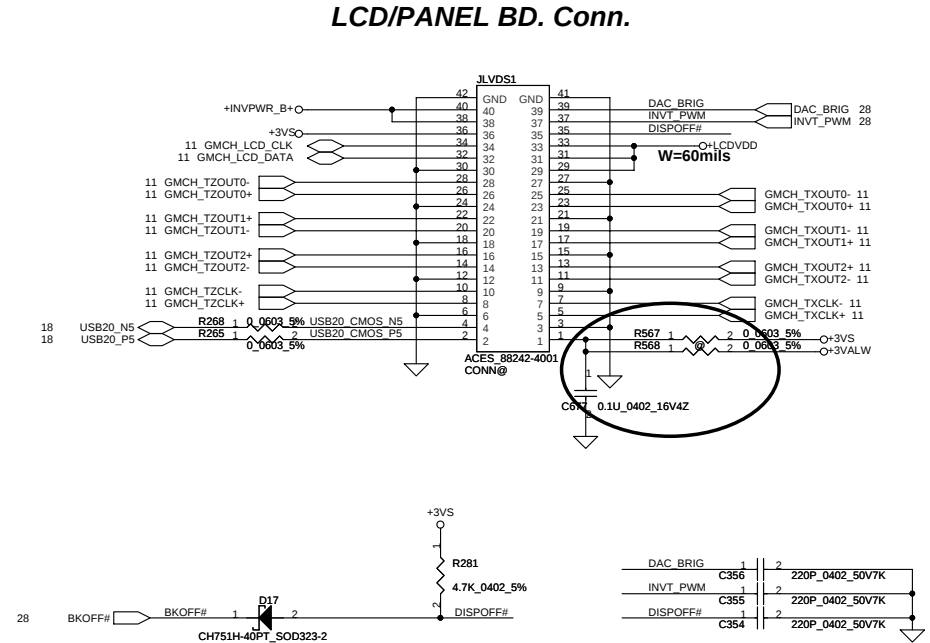
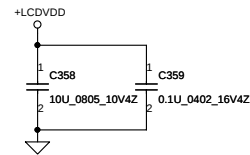
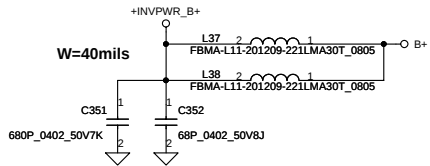
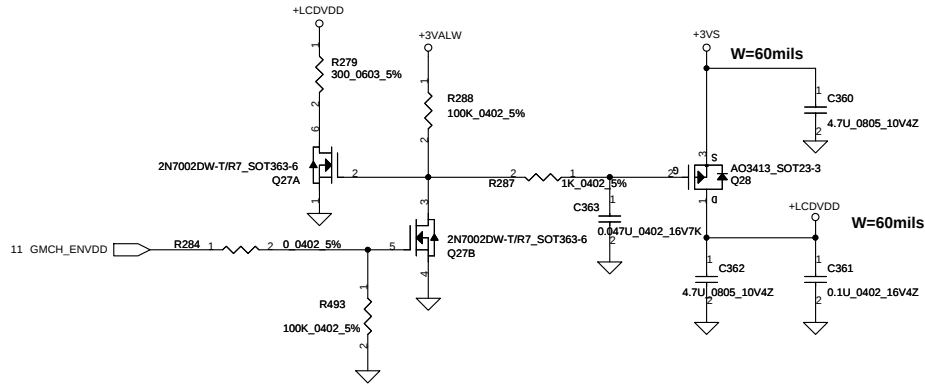
SRC 0	LAN
SRC 1	NEW CARD
SRC 2	MINI1 (WLAN)
SRC 3	
SRC 4	NB-Alink
SRC 5	CardReader
SRC 6	SB-Alink

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE (SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN		100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF (IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output
* default		

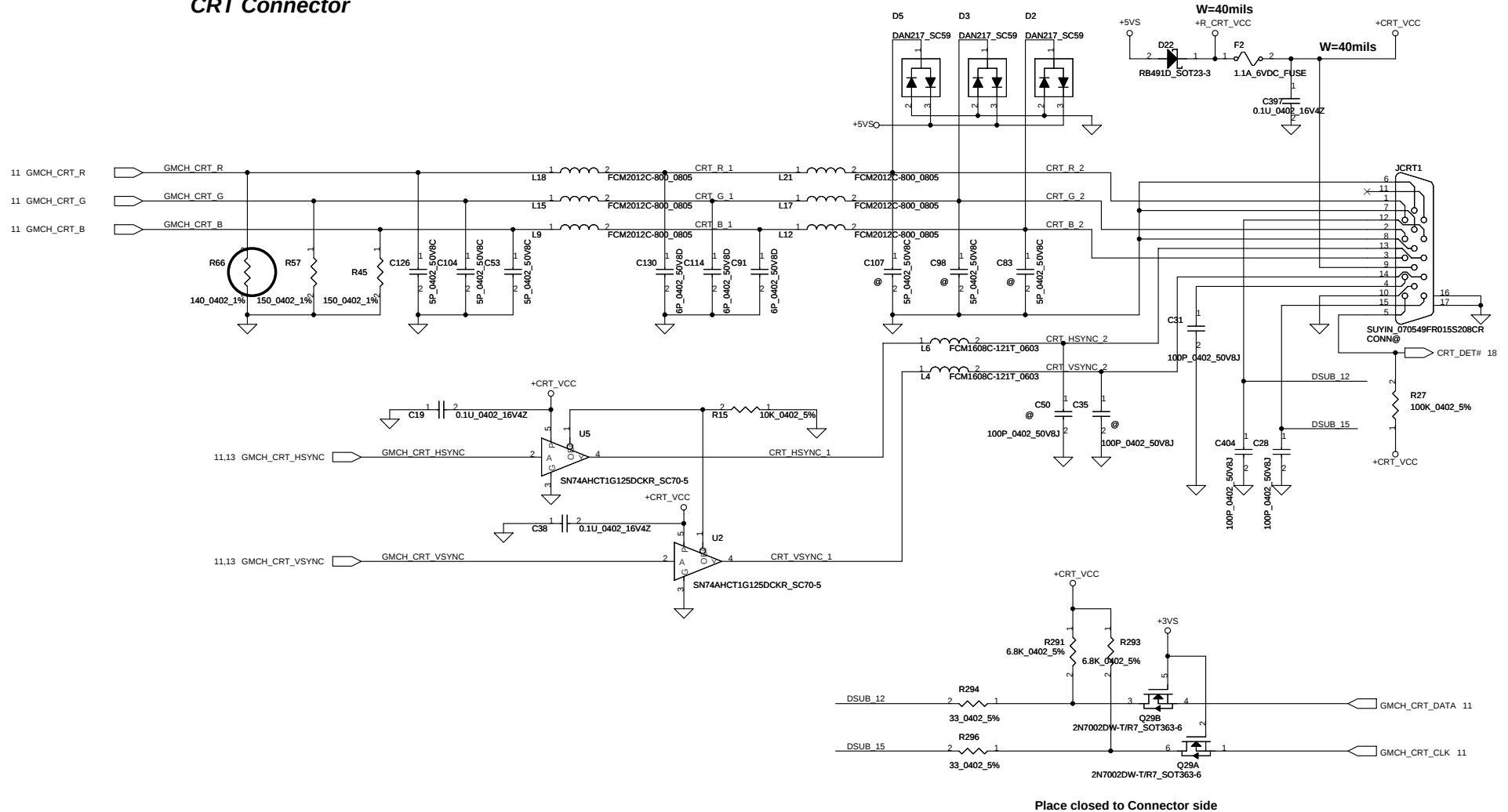
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LCD POWER CIRCUIT

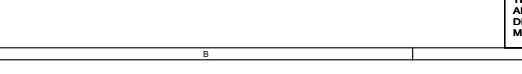
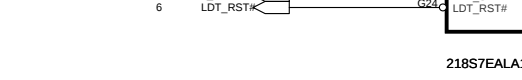
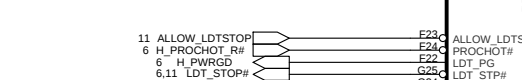
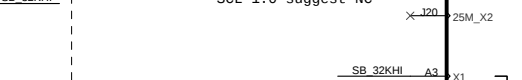
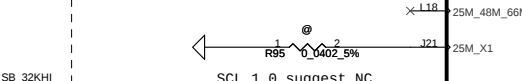
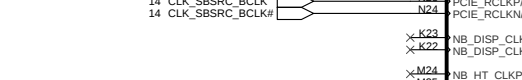
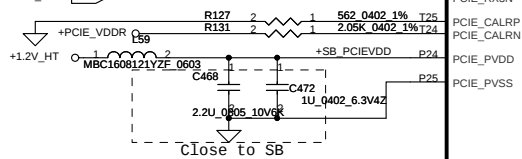
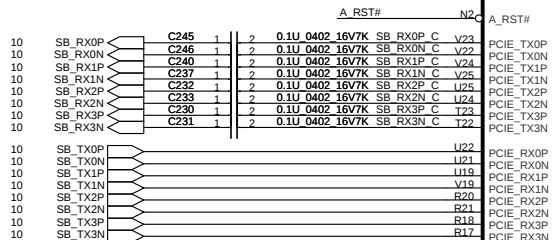
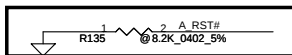


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CRT Connector



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SB700

Part 1 of 5

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

RTC XTAL

LPC

CPU

RTC

EC & Debug

STRAP PIN

for Clear CMOS

SECURITY CLASSIFICATION

ISSUED DATE

DECIPHERED DATE

TITLE

SCHEMATICS, MB A4391

DATE

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SCHEMATICS, MB A4391

Rev D

Document Number

401575

Rev D

Date

Tuesday, August 19, 2008

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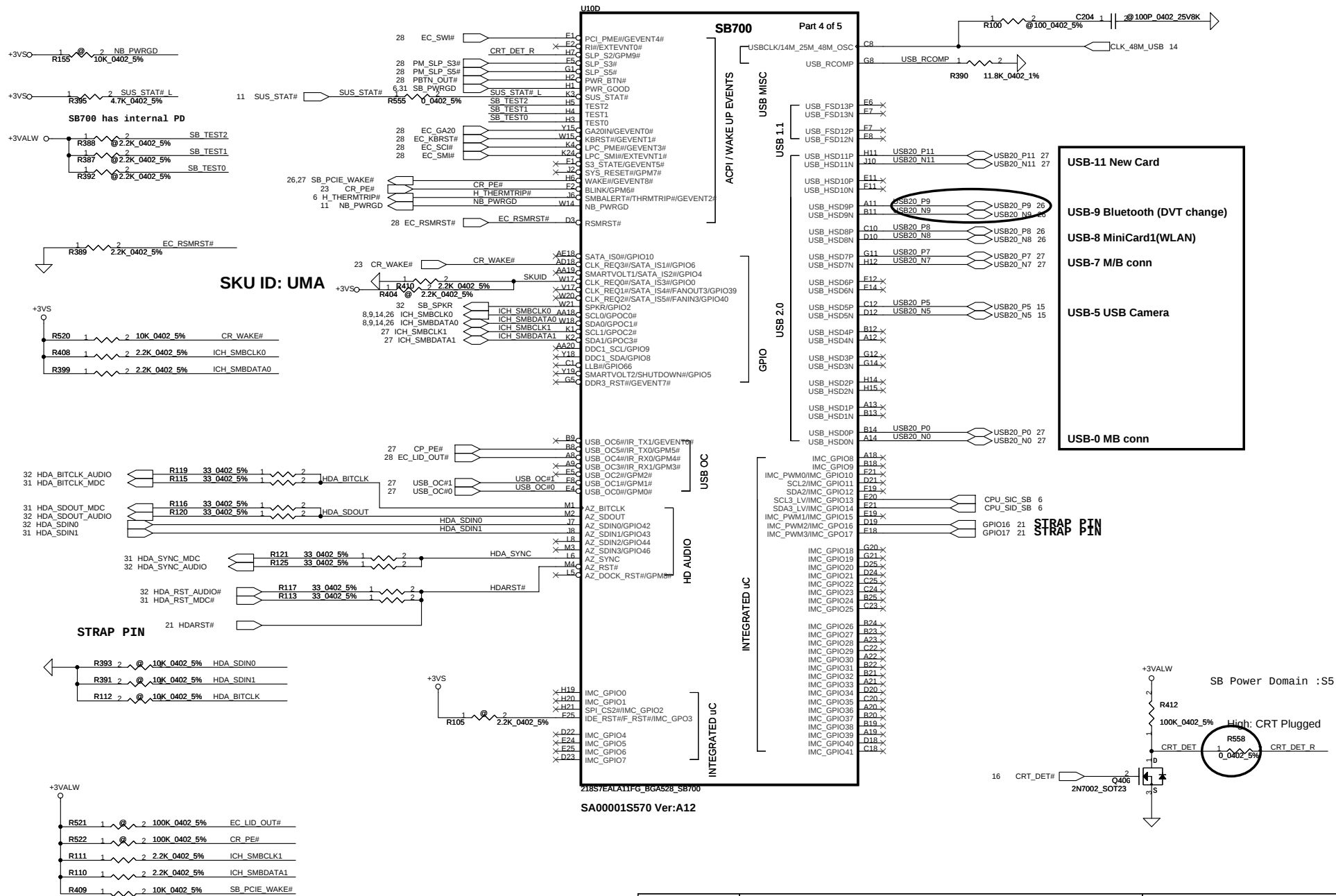
401575

Rev D

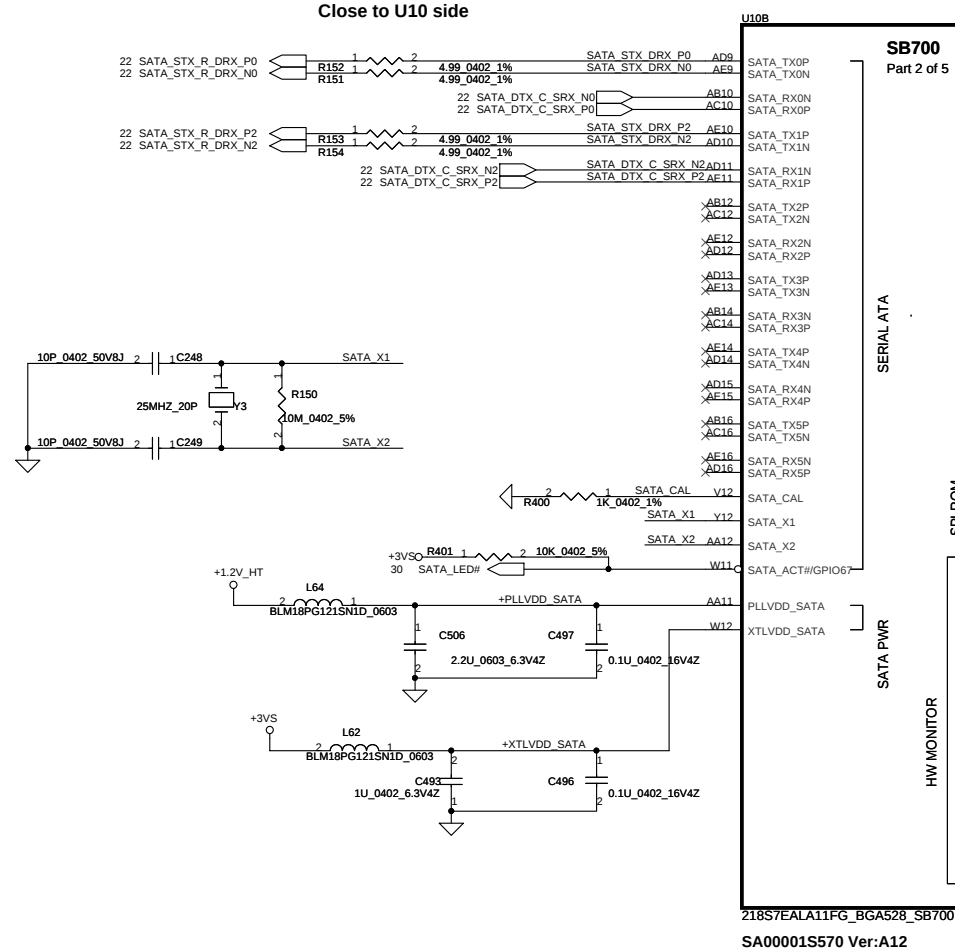
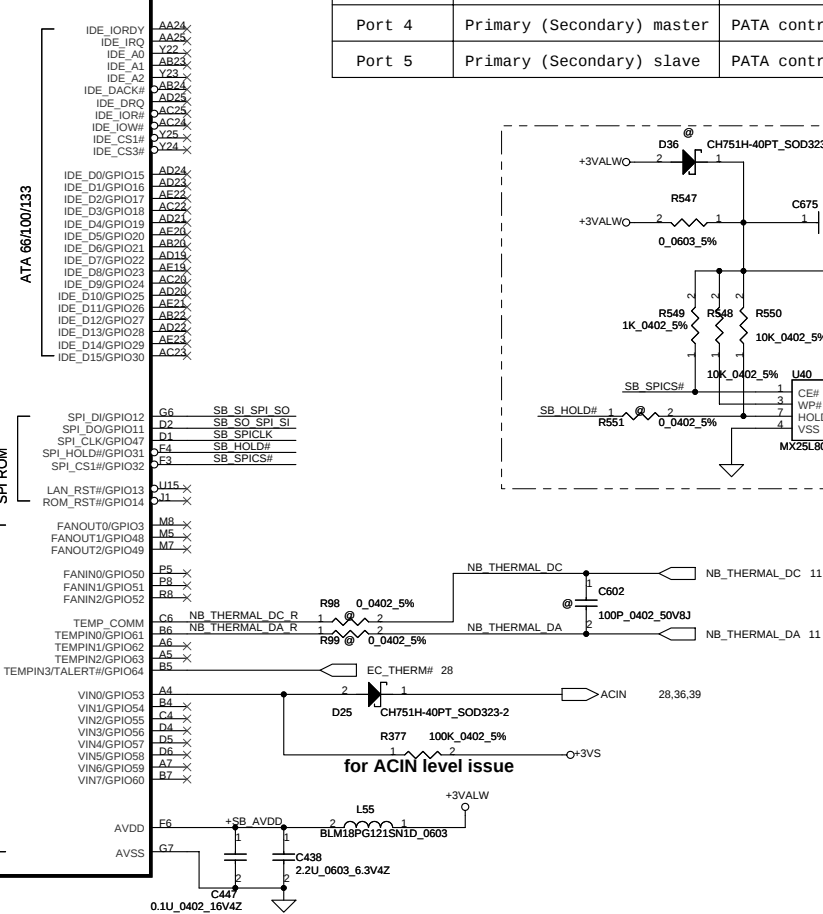
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Sheet



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[illegible]

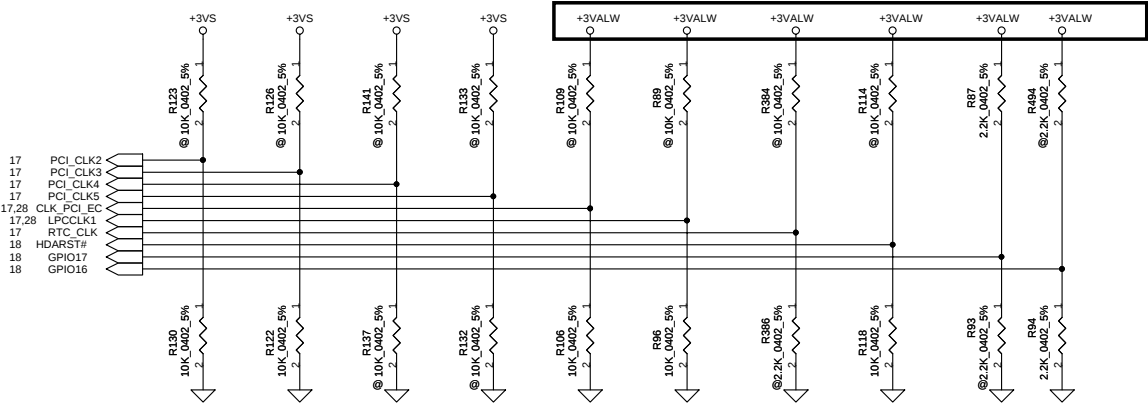
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

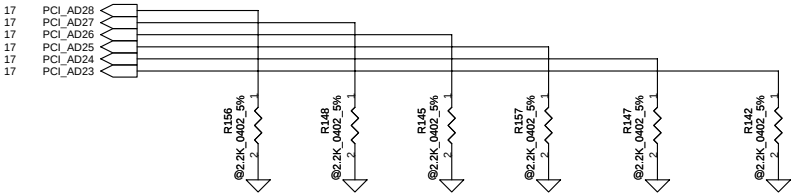
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	L,H = LPC ROM (Default L,NC) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		



DEBUG STRAPS

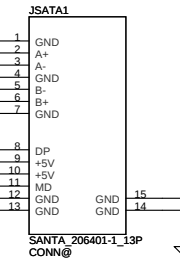
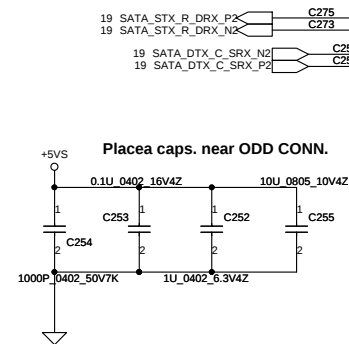
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



SATA ODD Conn.

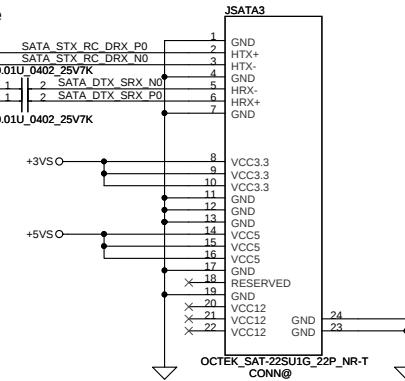
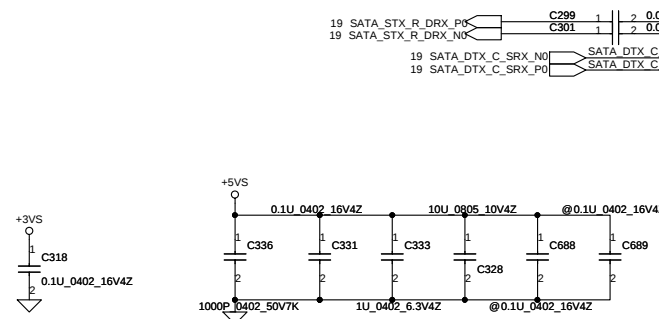
Close to Conn side



change footprint to Ring 5mm

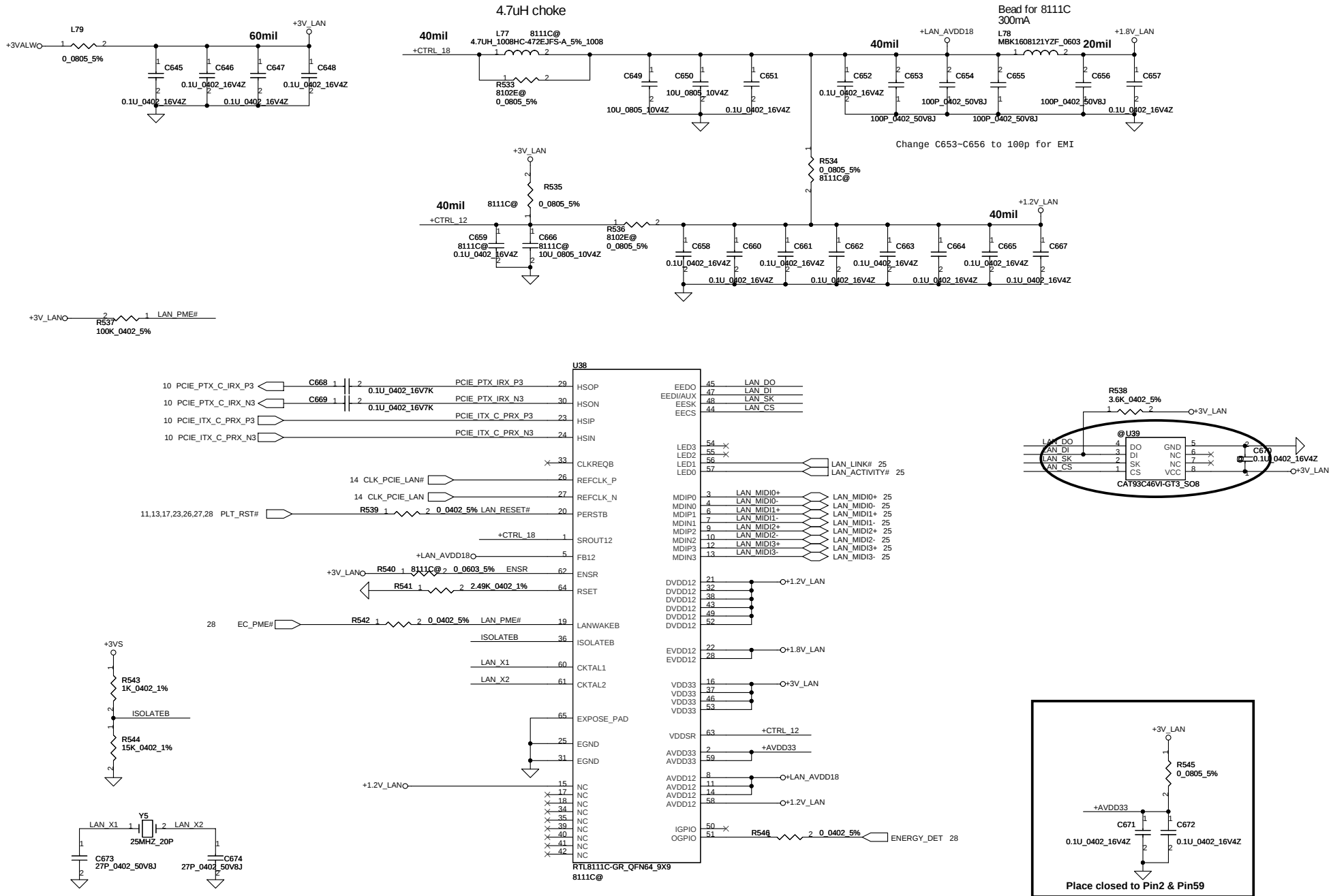
SATA HDD Conn.

Close to Conn side

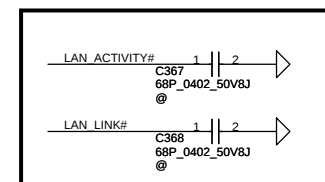
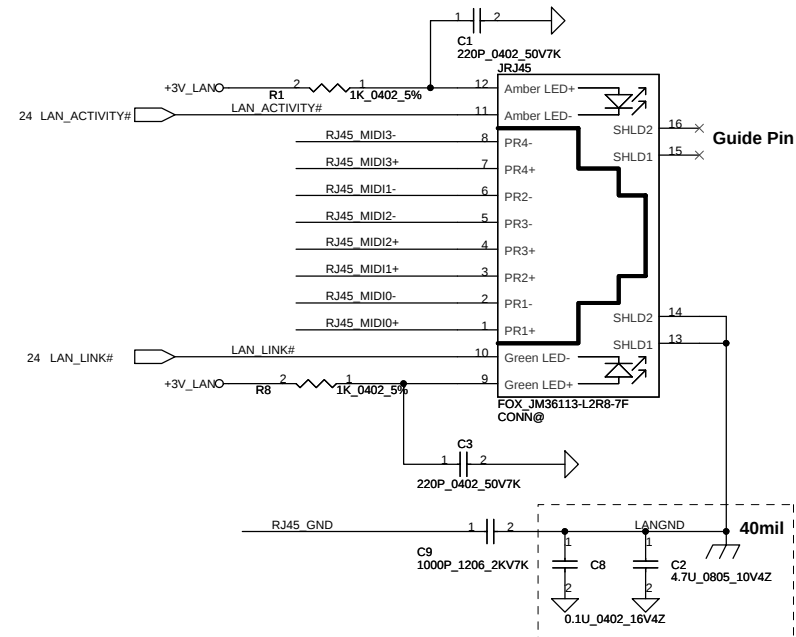
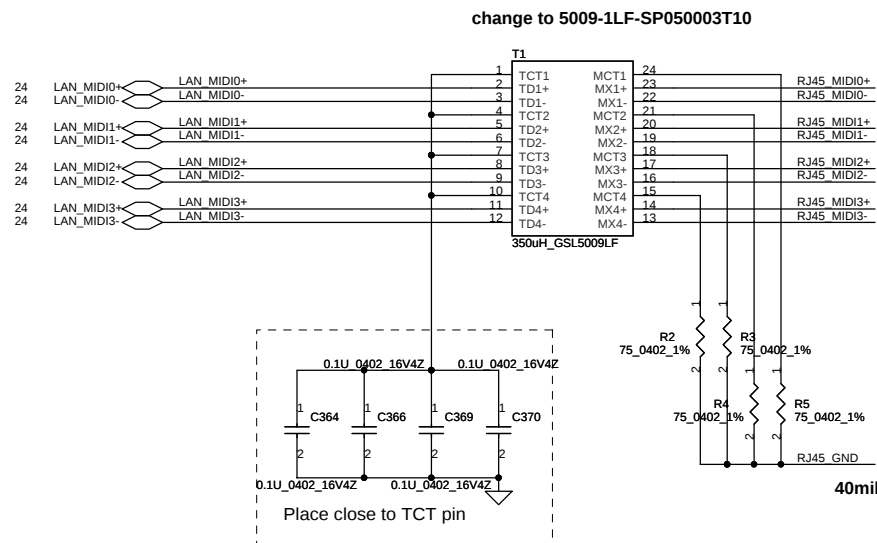


(JAL90 use)

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LAN RTL8111C/8102E

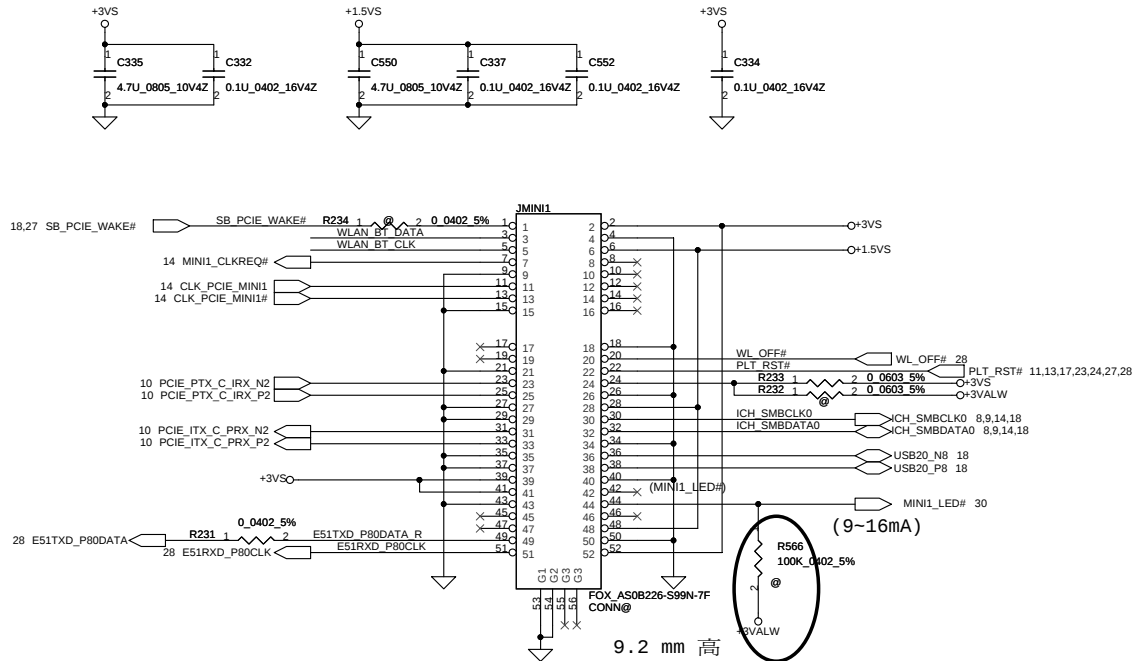
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For EMI

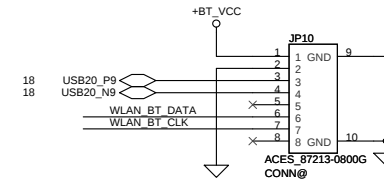
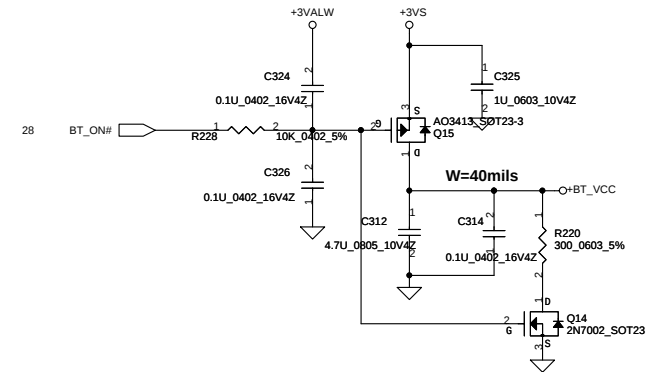
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For Wireless LAN



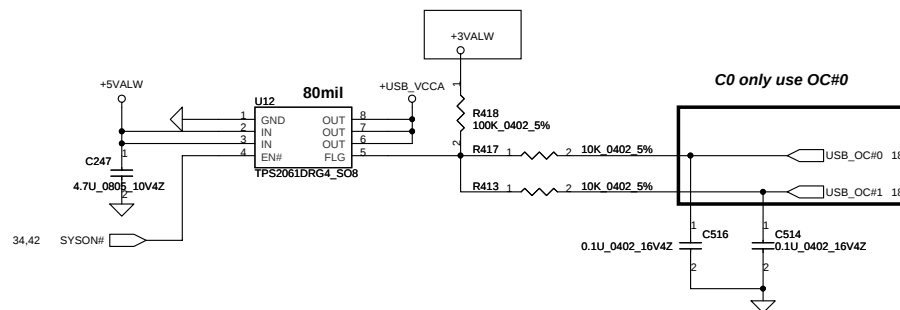
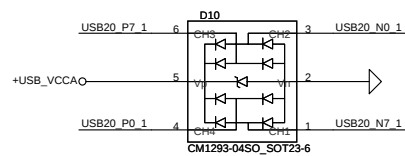
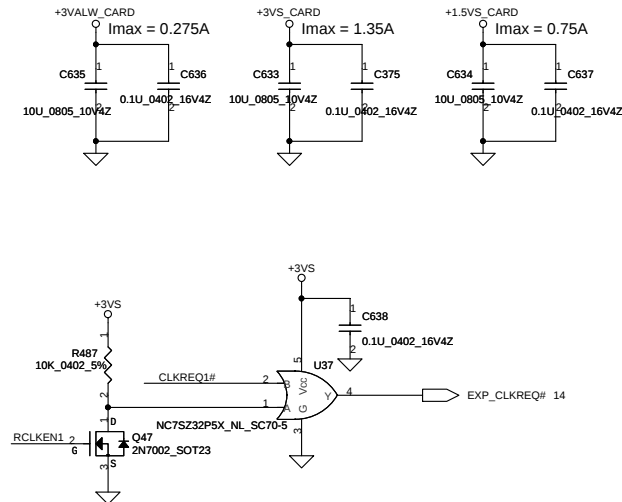
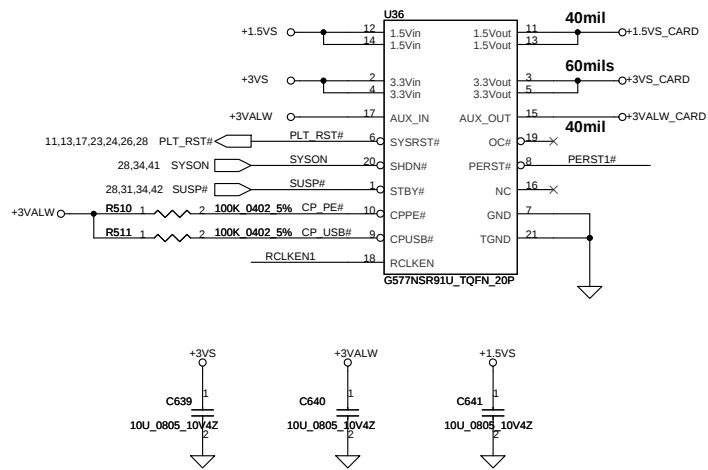
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Bluetooth Conn.

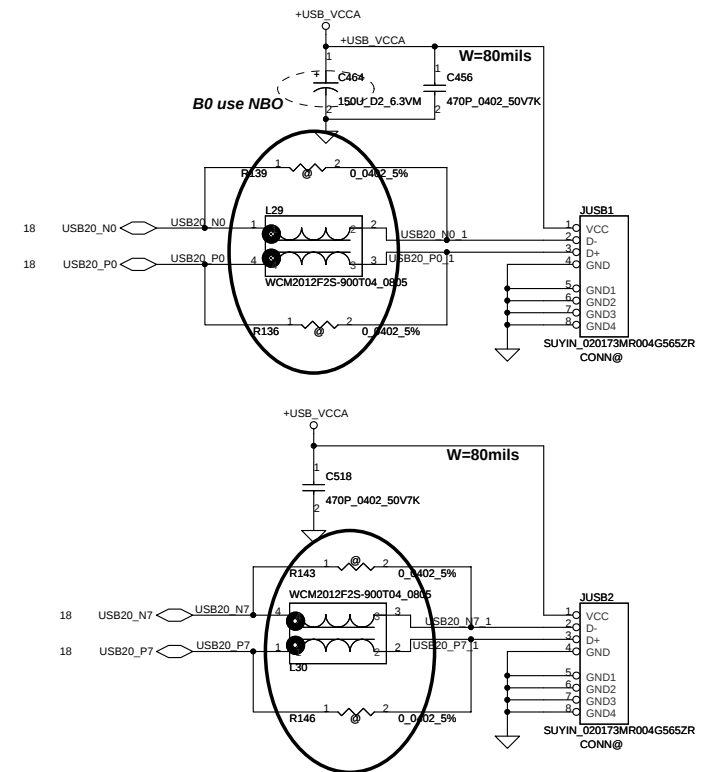
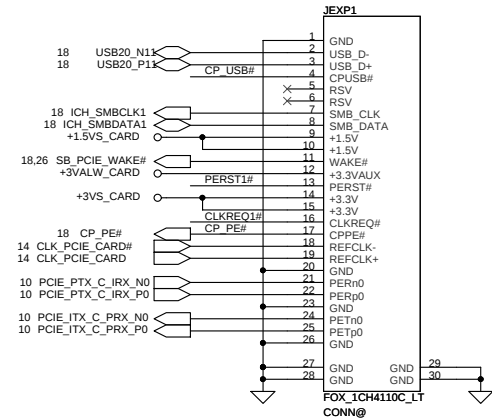


for 線材, 7, 8pin不打

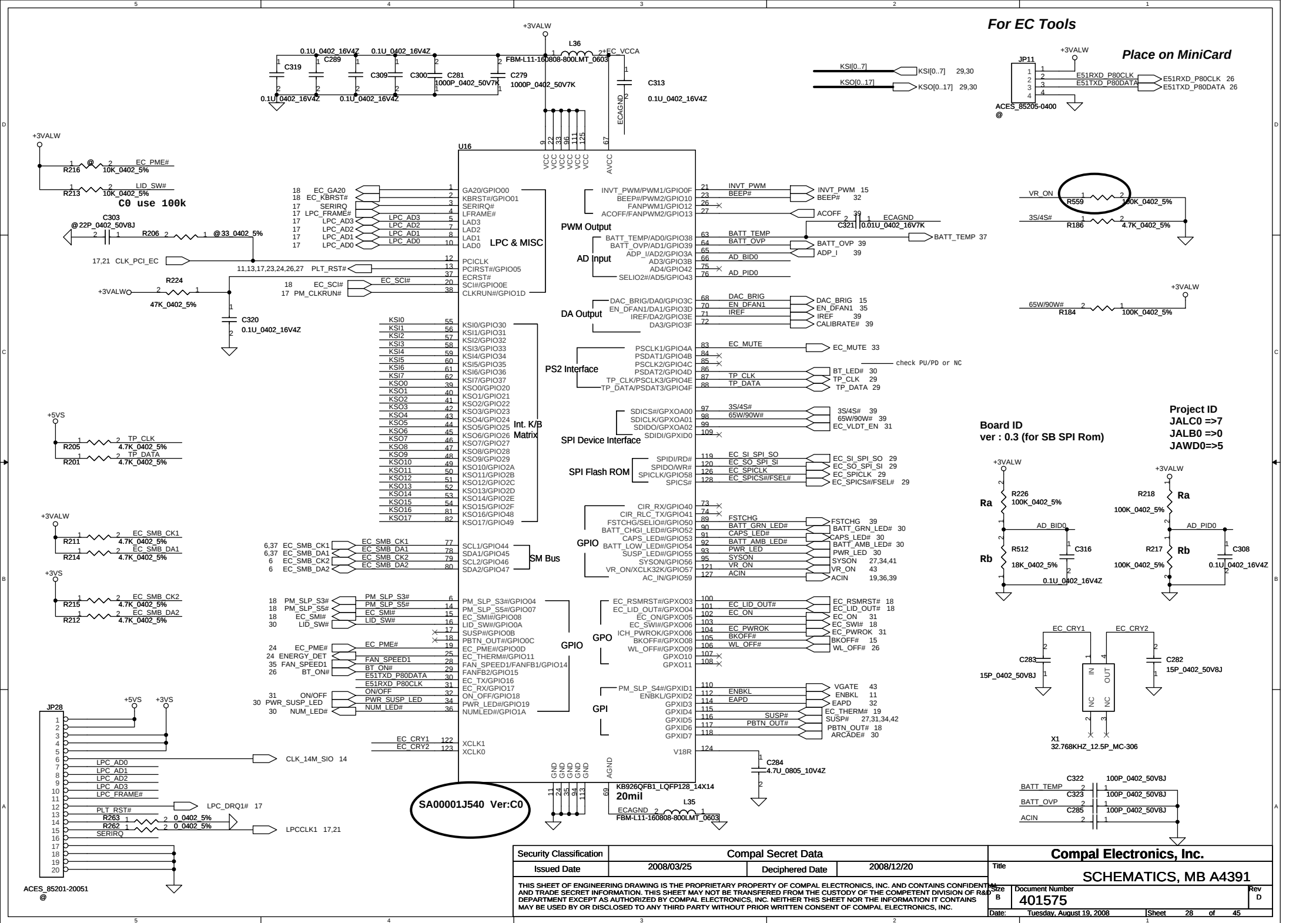
New Card Power Switch

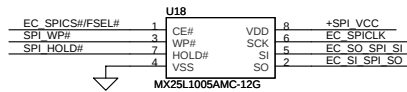
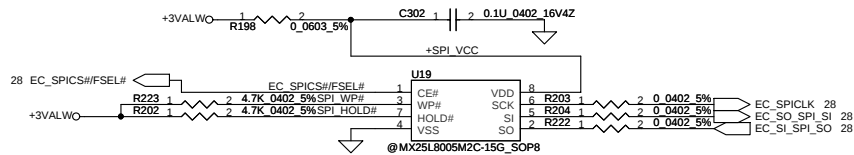


New Card Socket (Left/TOP)



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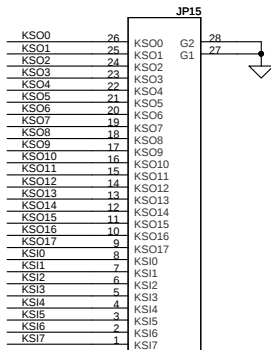




Reserved for BIOS simulator.
Footprint S08

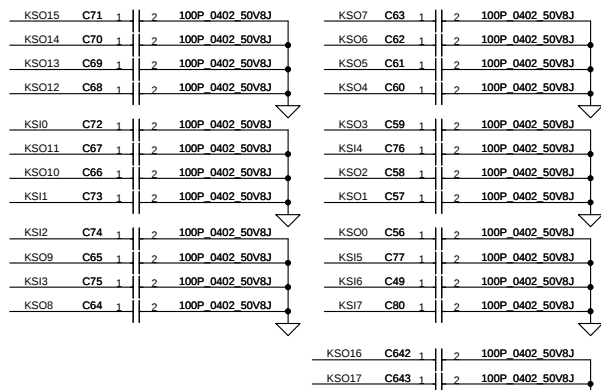
INT_KBD Conn.

(Left)

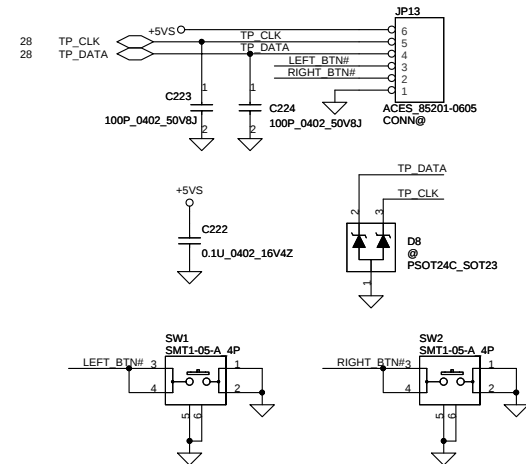


(Right)

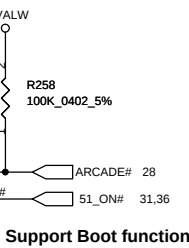
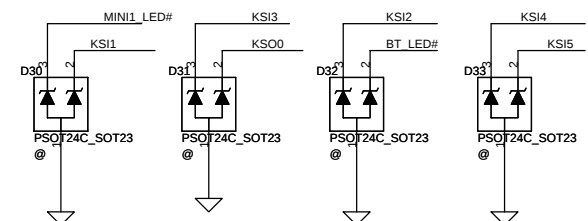
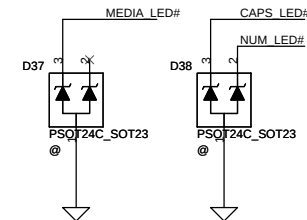
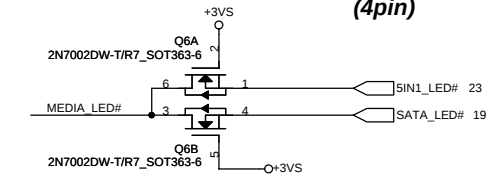
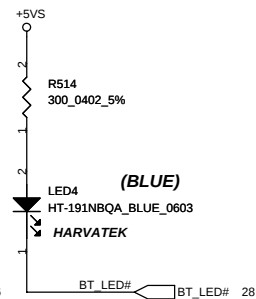
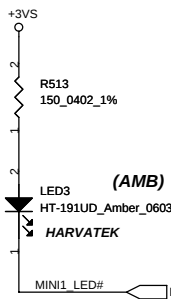
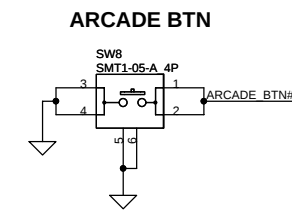
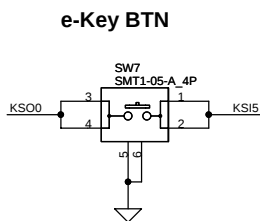
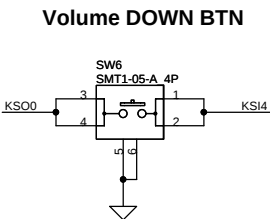
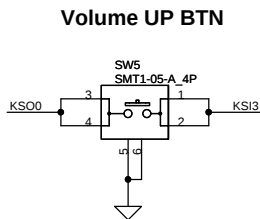
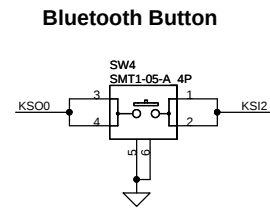
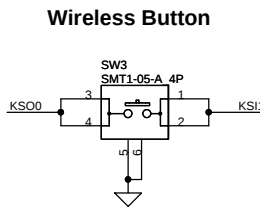
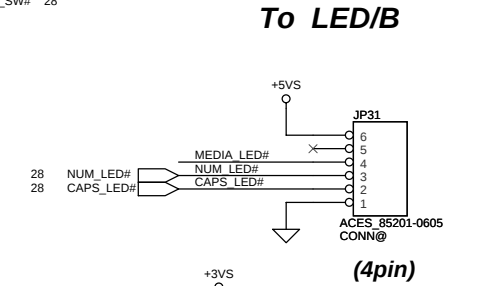
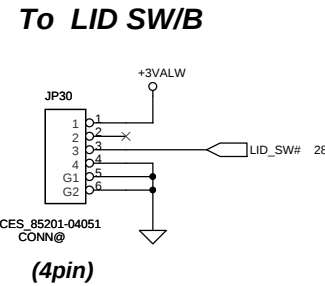
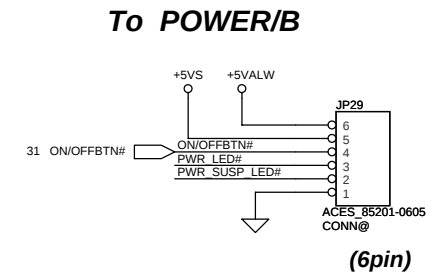
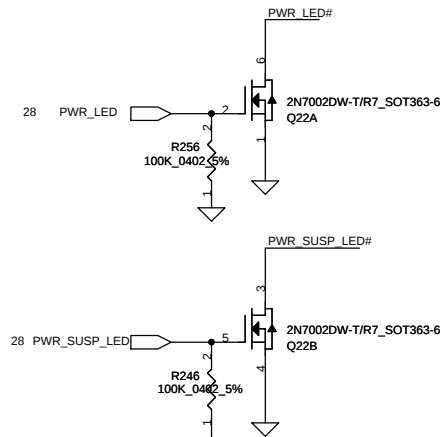
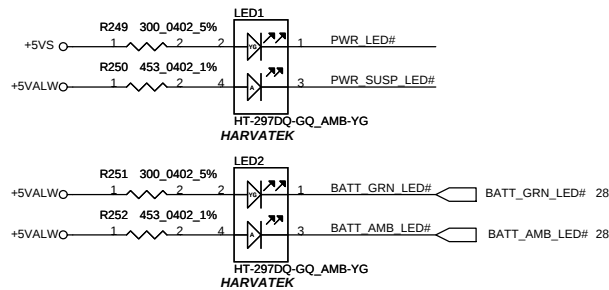
ACES_88747-2601
CONN@



To TP/B Conn.



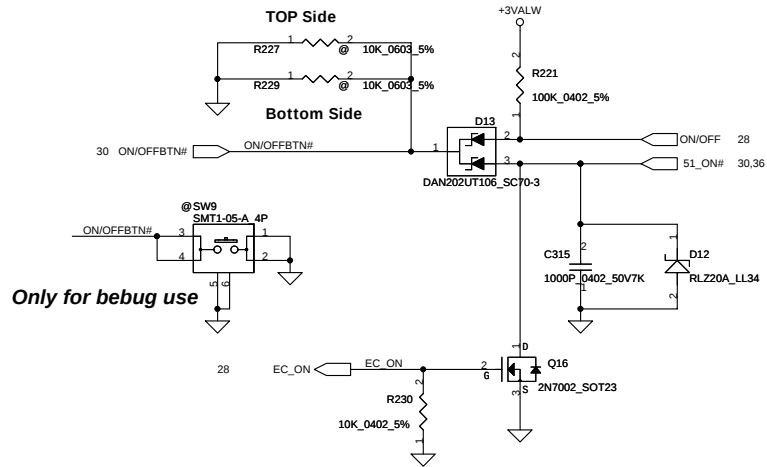
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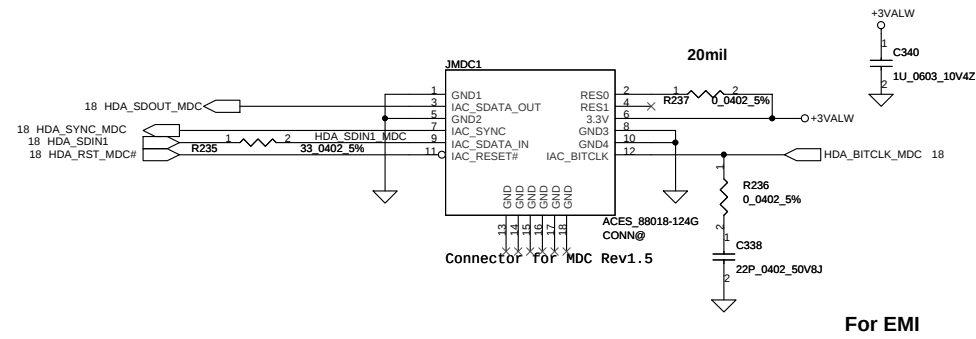
KSO0	
KSI1	Wireless BTN
KSI2	BT BTN
KSI3	Volume UP
KSI4	Volume DOWM
KSI5	e-Key BTN
KSI6	

Power Button

ON/OFF switch

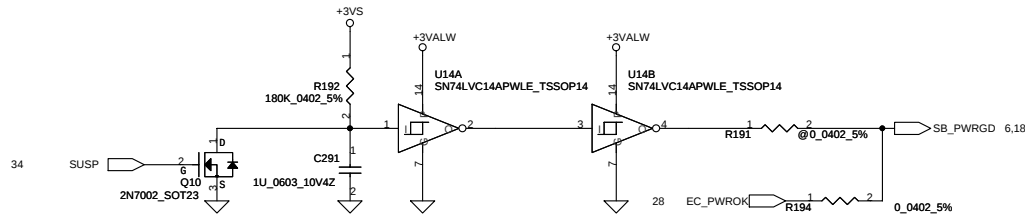


HDA MDC Conn.

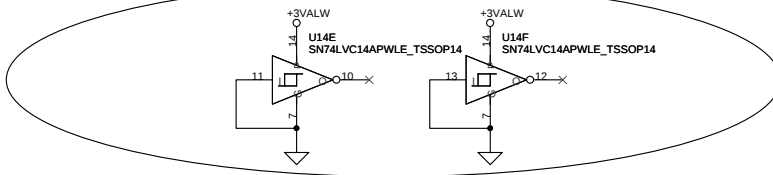
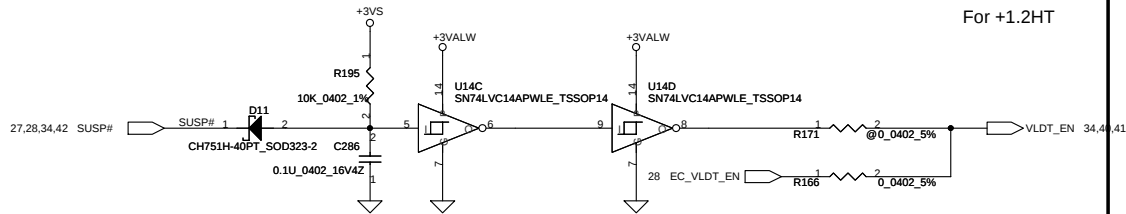


Power ON Circuit

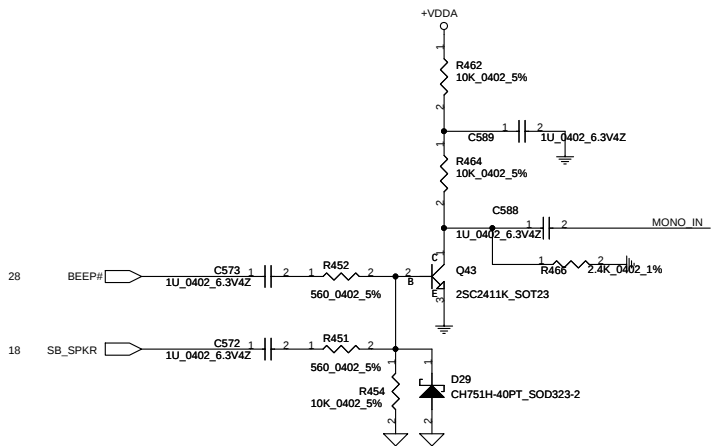
For South Bridge



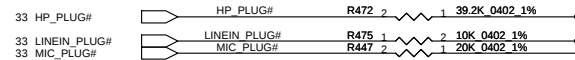
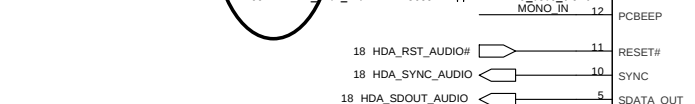
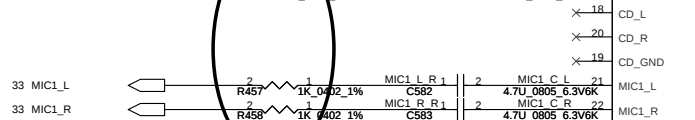
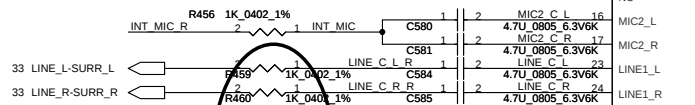
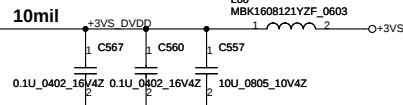
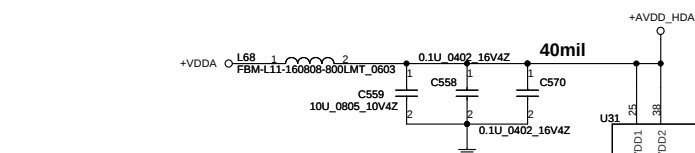
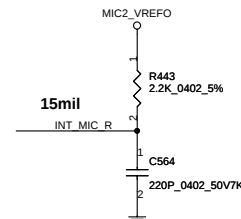
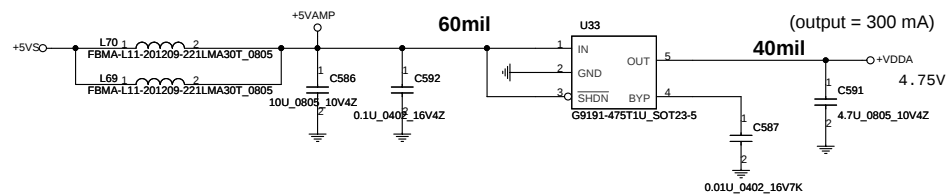
For +1.2HT



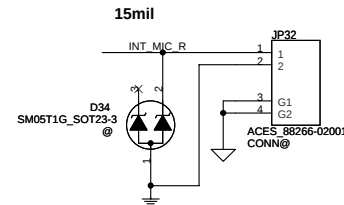
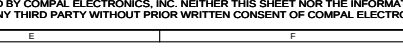
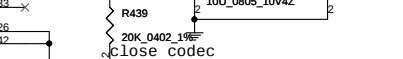
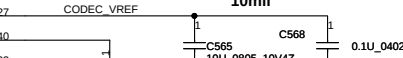
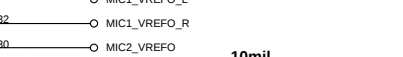
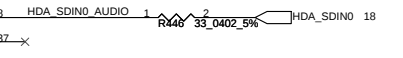
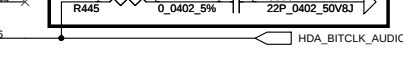
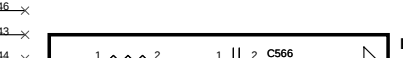
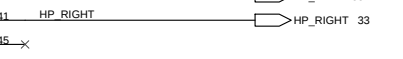
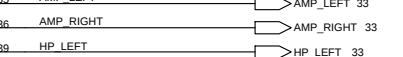
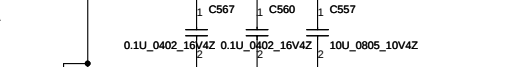
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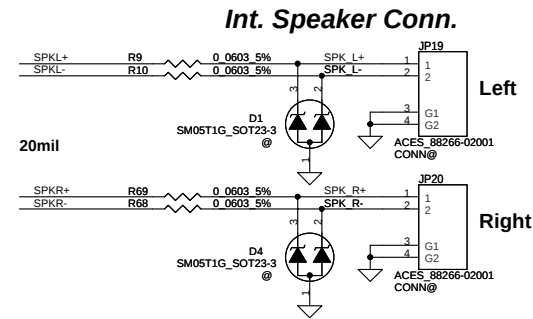
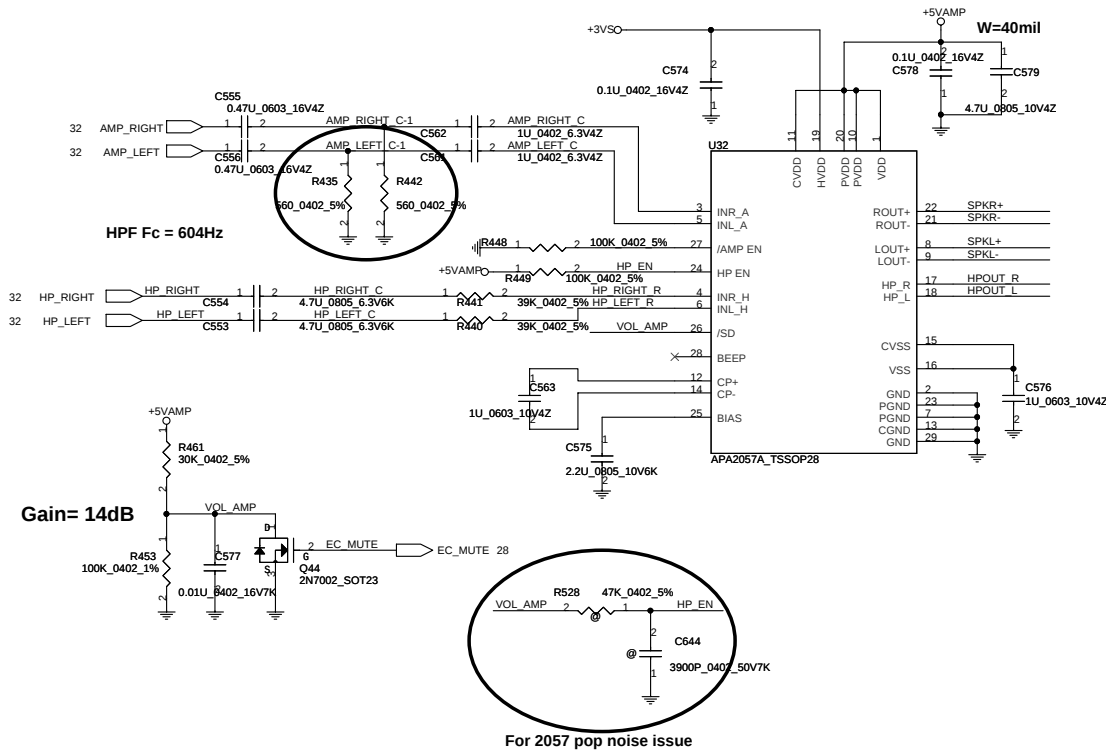
HD Audio Codec



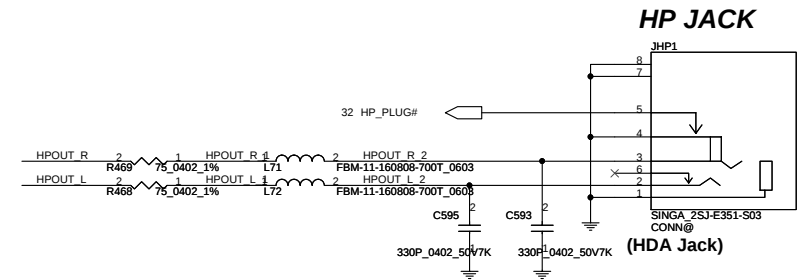
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



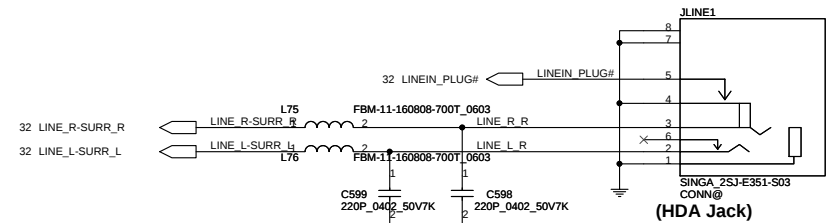
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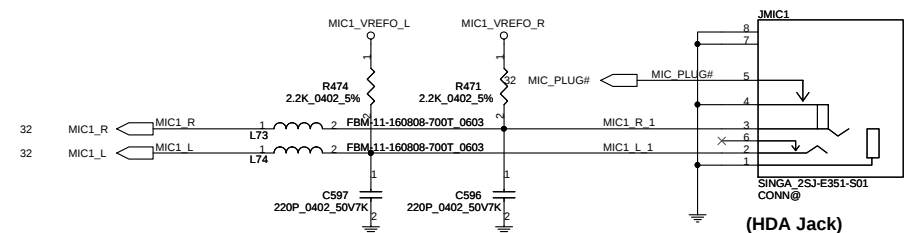
S/PDIF Out JACK LINE Out/Headphone Out



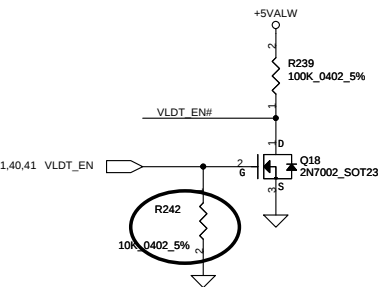
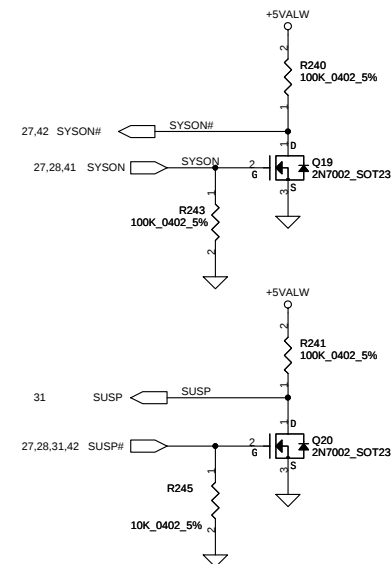
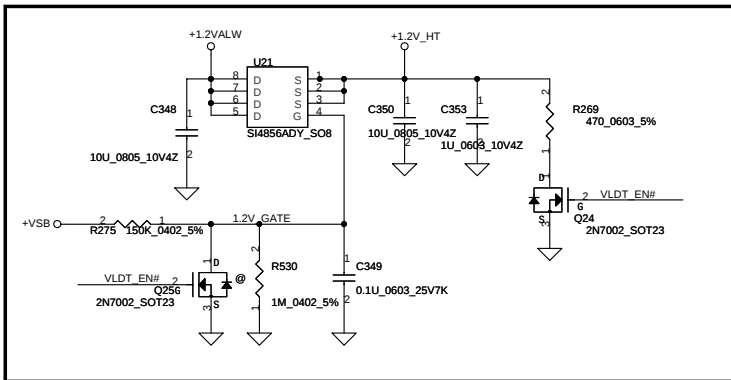
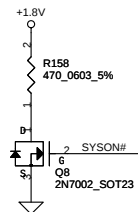
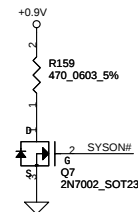
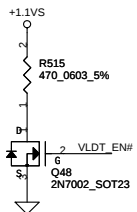
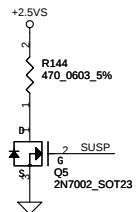
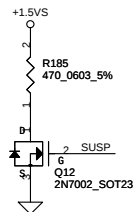
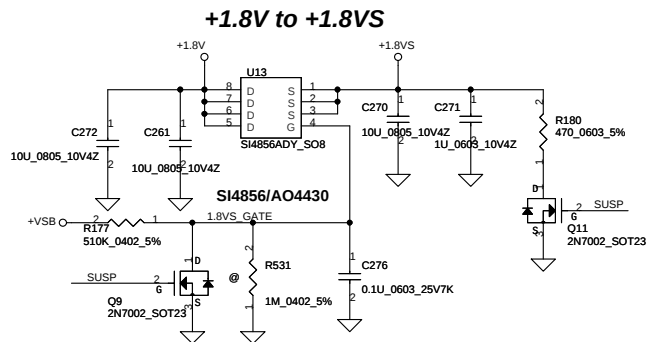
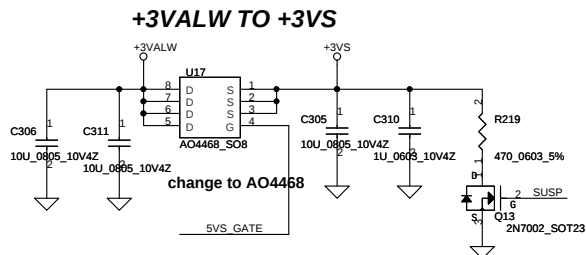
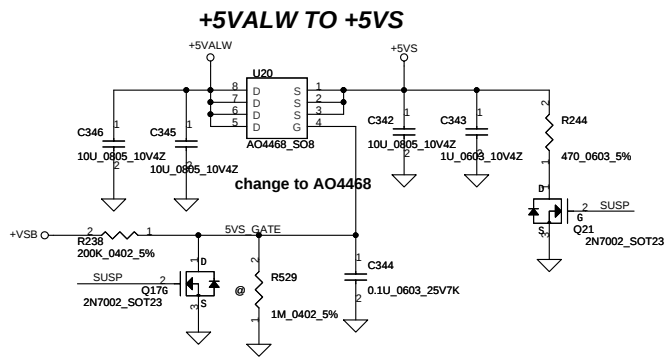
LINE-IN JACK



MIC JACK

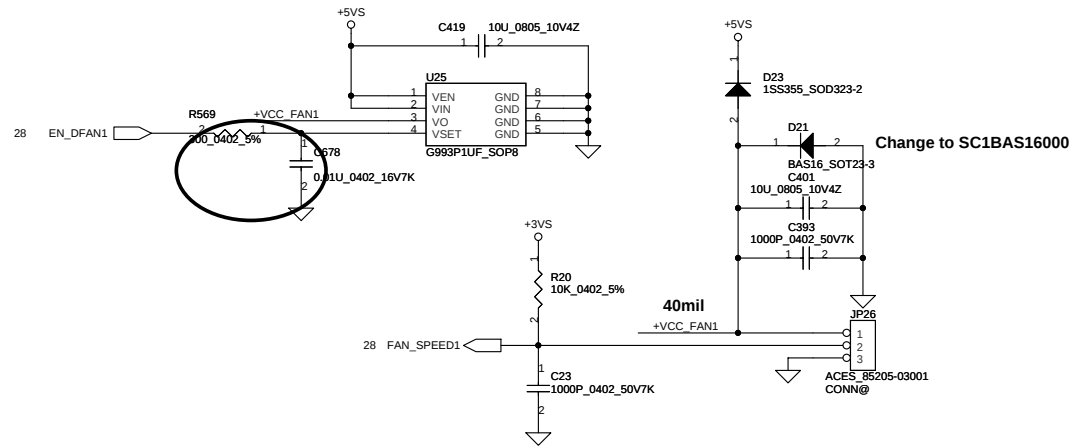


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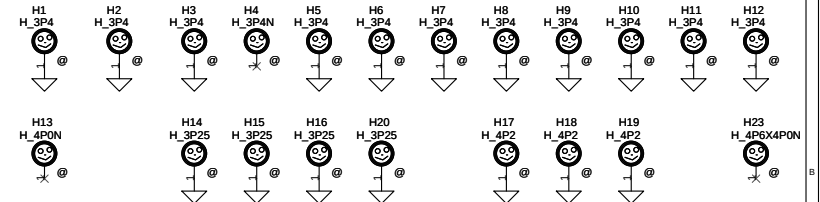
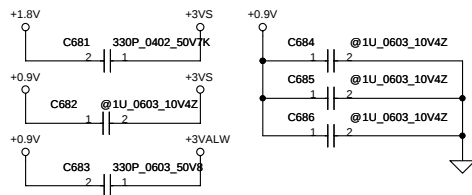


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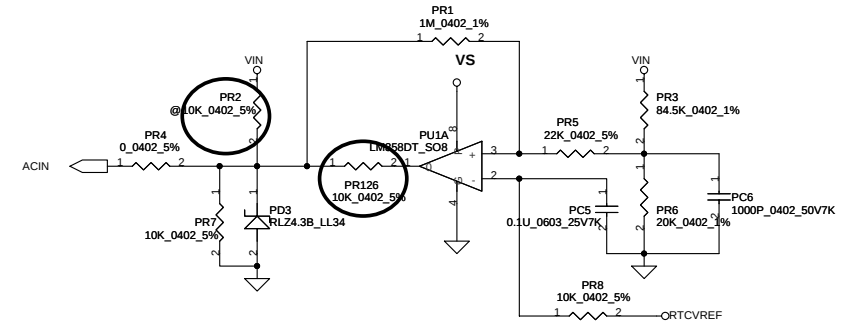
FAN1 Conn



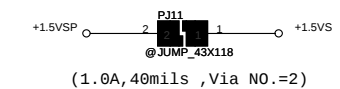
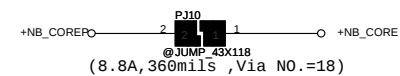
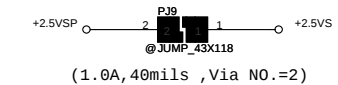
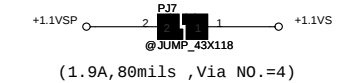
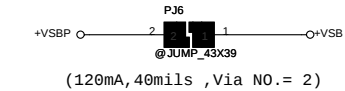
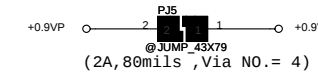
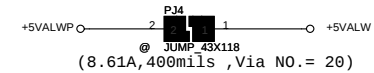
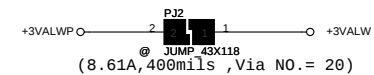
EMI solution



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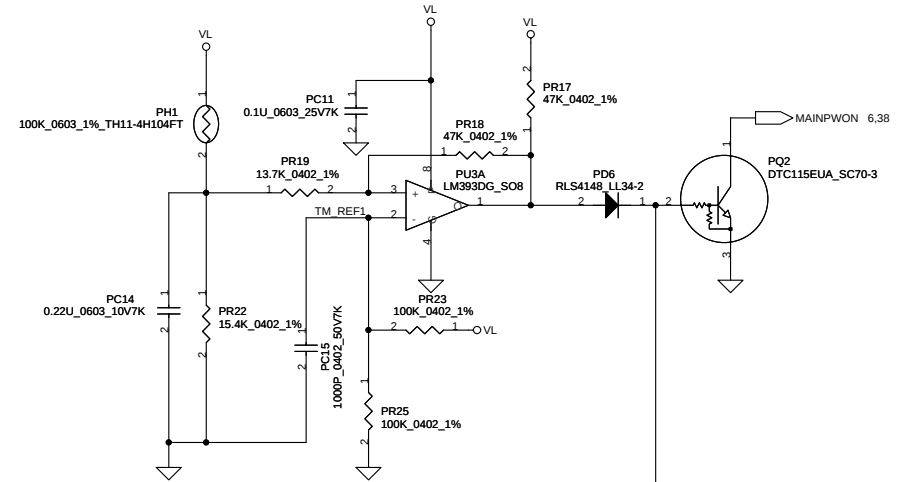
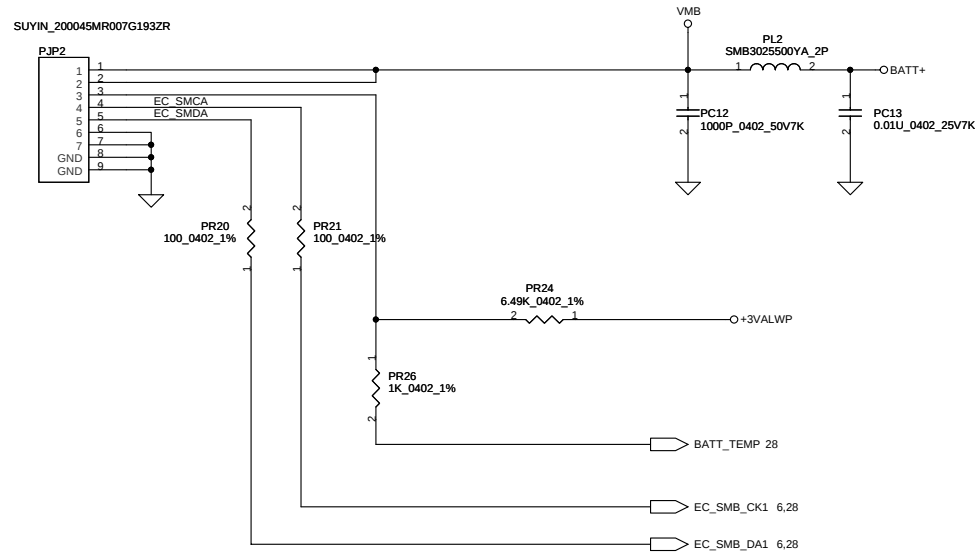


	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

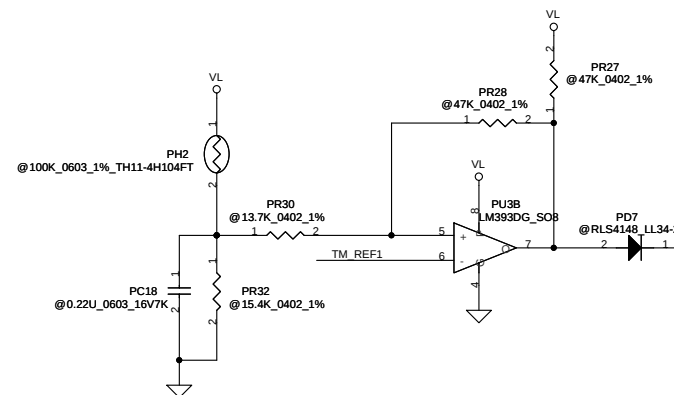
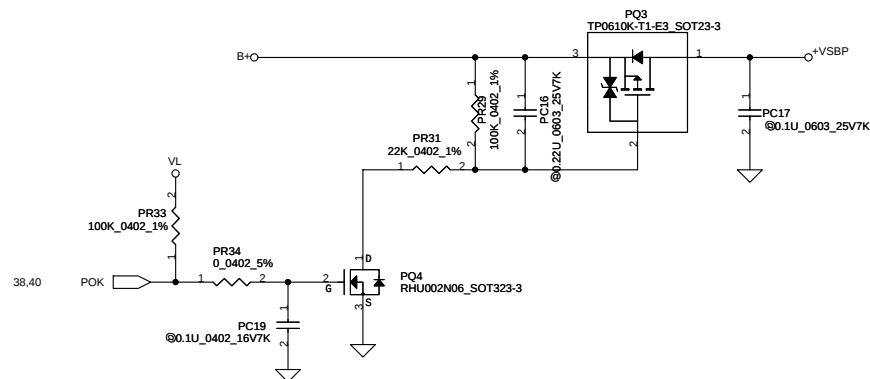


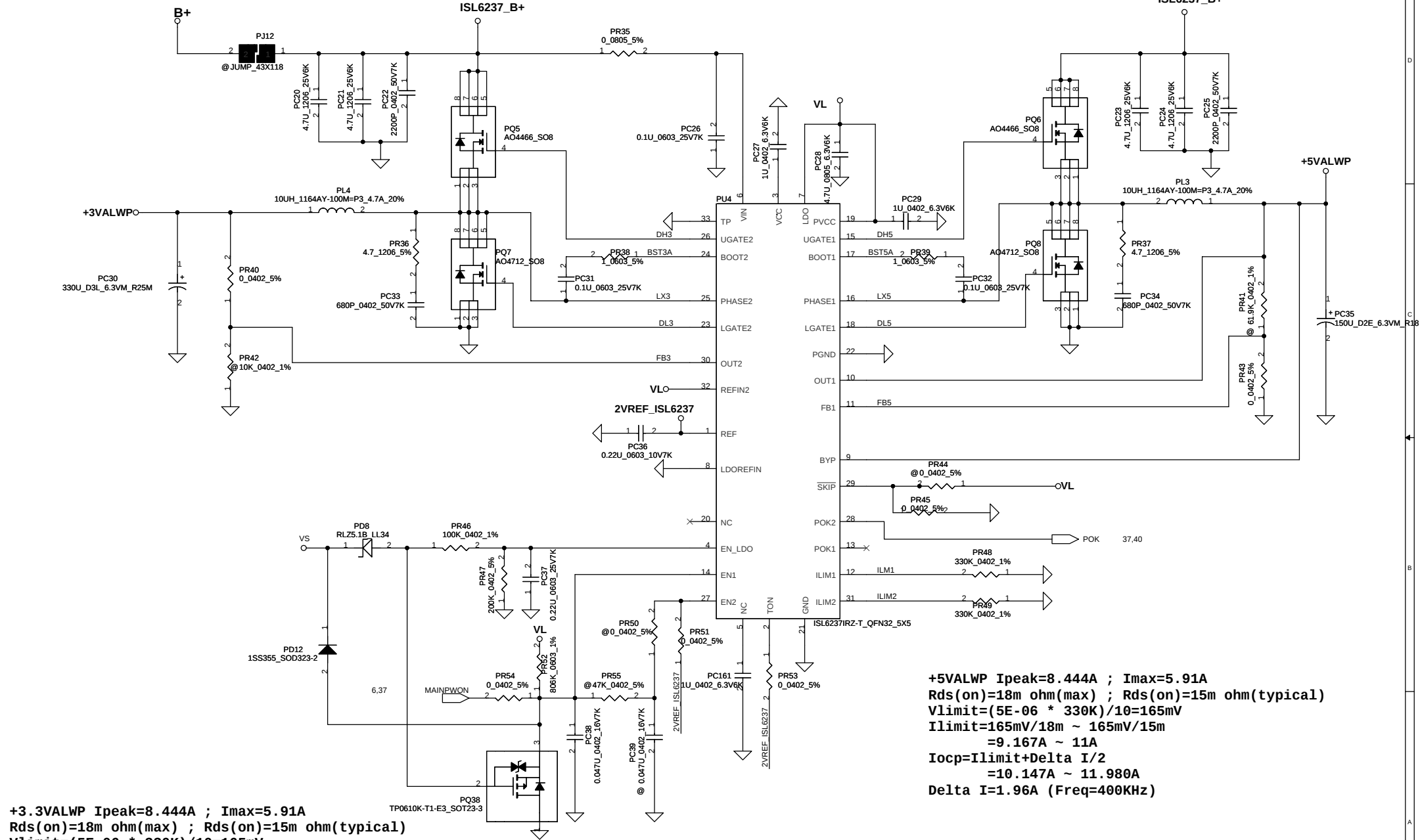
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PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

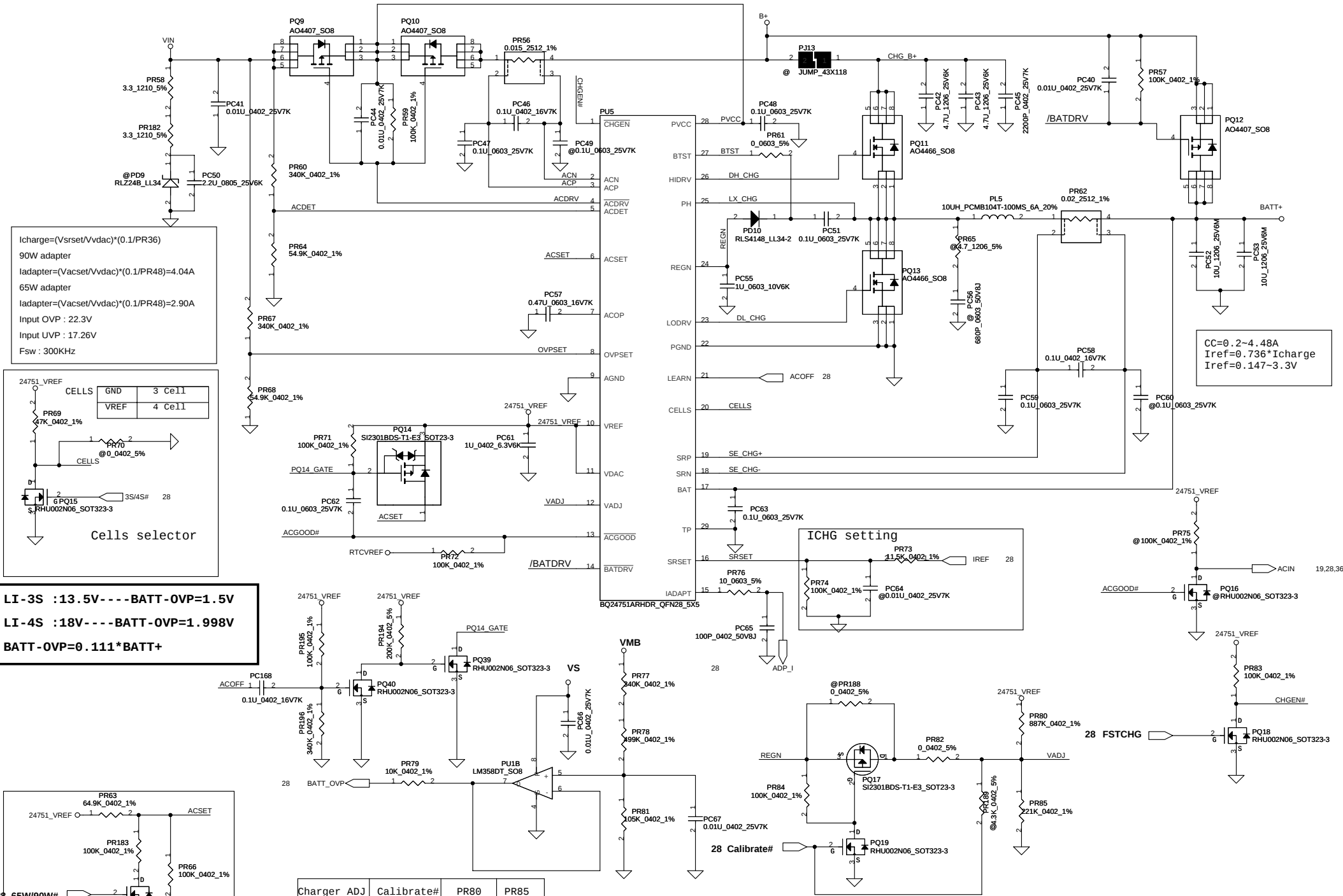


PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C

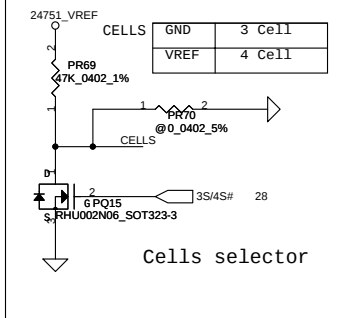




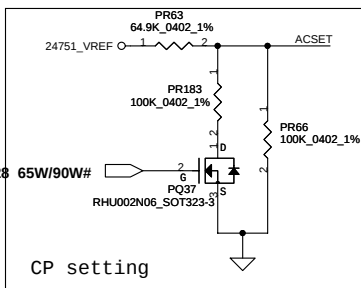
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$I_{charge} = (V_{srset} / V_{vdac}) * (0.1 / PR36)$
 90W adapter
 $I_{adapter} = (V_{acset} / V_{vdac}) * (0.1 / PR48) = 4.04A$
 65W adapter
 $I_{adapter} = (V_{acset} / V_{vdac}) * (0.1 / PR48) = 2.90A$
 Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz



LI-3S :13.5V---BATT-OVP=1.5V
LI-4S :18V---BATT-OVP=1.998V
BATT-OVP=0.111*BATT+



1.1V Ipeak=8.9A ; Imax=6.23A
DCR=6m ohm (max)
Rocset=(Iocp*DCR)/10E-06=7.87K ohm
Iocp=10.089A(1.3*DCR)
Csen=L/(Rocset*DCR)=0.022uF

Freq=303KHz
Rfset=1/(1.5E-10 * Freq)=22K

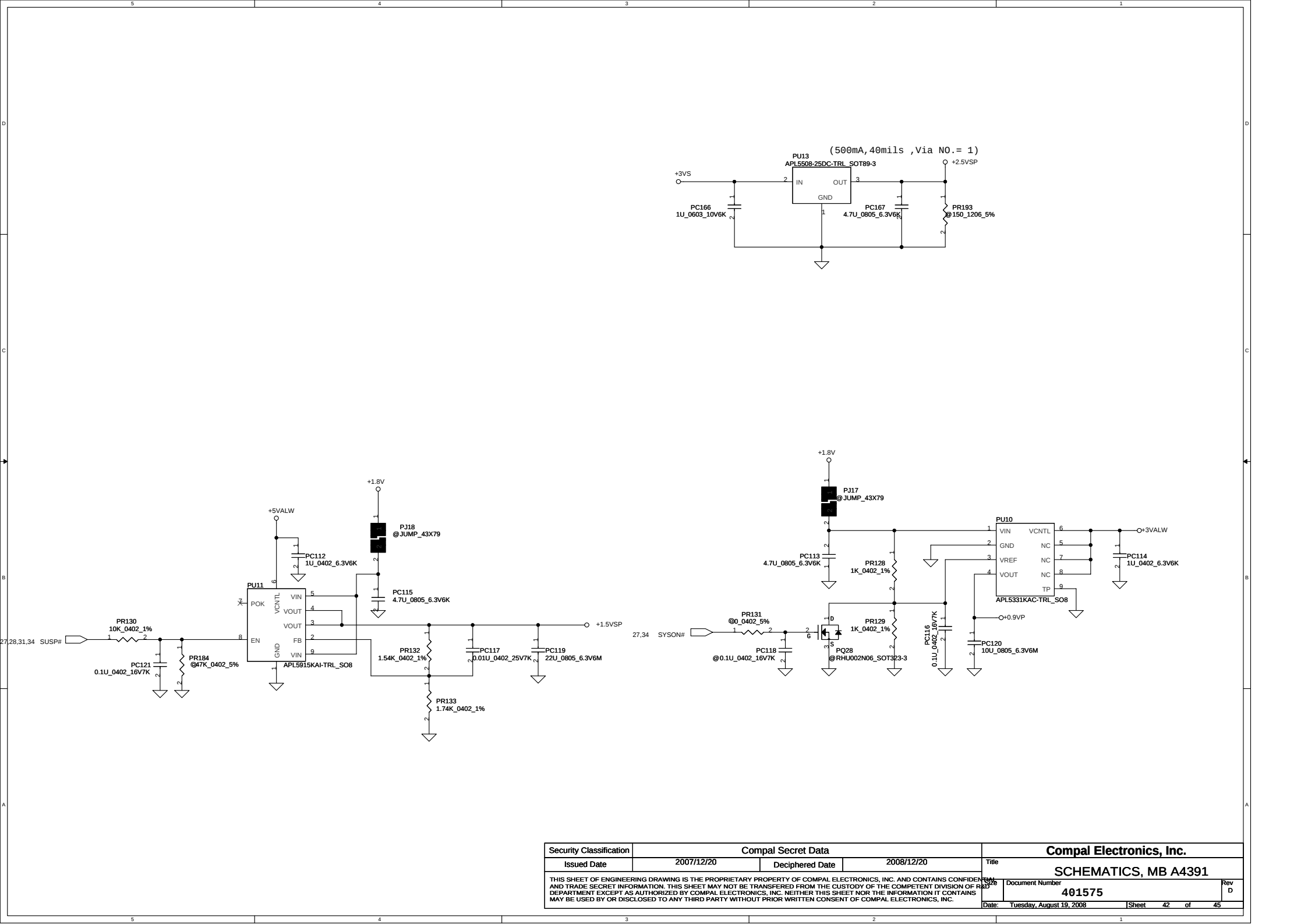
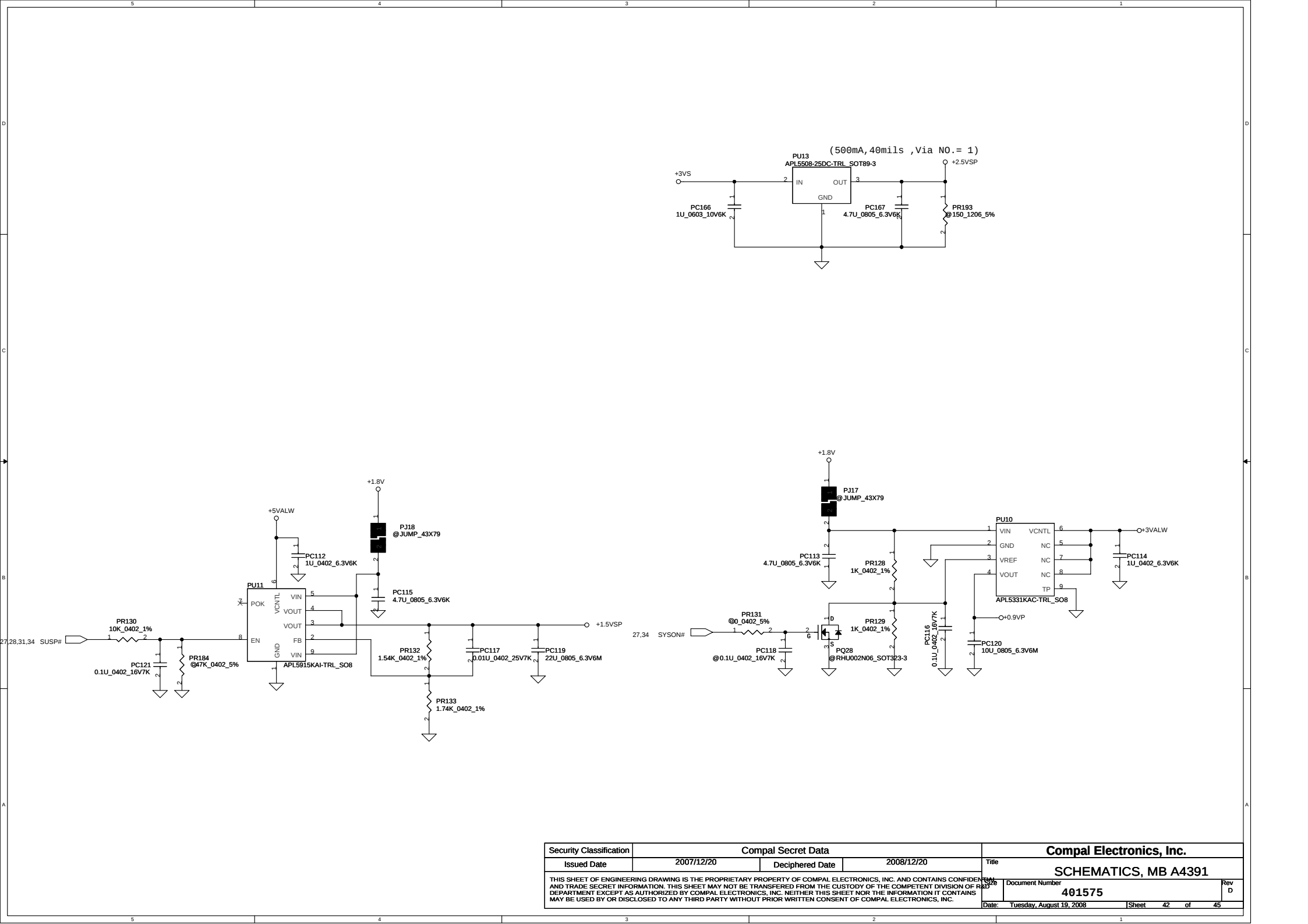
1.2VP Ipeak=3.94A ; Imax=2.758A
DCR=10m ohm (max)
Rocset=(Iocp*DCR)/10E-06=8.06K ohm
Iocp=6.716A(1.2*DCR)
Csen=L/(Rocset*DCR)=0.022uF

Freq=366KHz
Rfset=1/(1.5E-10 * Freq)=18.2K

1.2VP Ipeak=3.94A ; Imax=2.758A
DCR=10m ohm (max)
Rocset=(Iocp*DCR)/10E-06=8.06K ohm
Iocp=6.716A(1.2*DCR)
Csen=L/(Rocset*DCR)=0.022uF

Freq=366KHz
Rfset=1/(1.5E-10 * Freq)=18.2K

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[illegible]

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	Add NB_CORE B+ circuit	NB_CORE B+ 加強	0.1	40	Add PL14 SM010016410 (S SUPPRE_ KC FBMA-L11-322513-151LMA50T)	20080506	PVT
2	Modify the circuit for Vin dectector	BOM modify	0.1	36	Cahnge PR122 SD028100280(S RES 1/16W 10K +-5% 0402) to PR126 SD028100280(S RES 1/16W 10K +-5% 0402)	20080506	PVT
3	1.1V circuit change	For debug	0.1	41	Add PU8 SA000015410 (S IC APL5912-KAC-TRL SO 8P LDO)	20080506	PVT
4	1.1V circuit change	For debug	0.1	41	Add PC102 SE000000K80(S CER CAP 1U 6.3V K X5R 0402)	20080506	PVT
5	1.1V circuit change	For debug	0.1	41	Add PC103 SE093475K80 (S CER CAP 4.7U 6.3V K X5R 0805 H1.25)	20080506	PVT
6	1.1V circuit change	For debug	0.1	41	Add PC104 SE075103K80 (S CER CAP .01U 25V K X7R 0402)	20080506	PVT
7	1.1V circuit change	For debug	0.1	41	Add PC105 SE000000I10 (S CER CAP 22UF 6.3V M X5R 0805 H1.25)	20080506	PVT
8	1.1V circuit change	For debug	0.1	41	Add PC106 SE000000K80 (S CER CAP 1U 6.3V K X5R 0402)	20080506	PVT
9	1.1V circuit change	For debug	0.1	41	Add PR122 SD034120280 (S RES 1/16W 12K +-1% 0402)	20080506	PVT
10	1.1V circuit change	For debug	0.1	41	Add PR123 SD034115180 (S RES 1/16W 1.15K +-1% 0402)	20080506	PVT
11	1.1V circuit change	For debug	0.1	41	Add PR124 SD034300180 (S RES 1/16W 3K +-1% 0402)	20080506	PVT
12	NB_CORE low side MOS change	BOM modify	0.1	40	Cahnge PQ24 SB000000AJ00(S TR AO4712 1N SO8) to SB0000004T80(S TR FDS6670AS_NL 1N SO8)	20080506	PVT
13	1.8V low side MOS change	BOM modify	0.1	41	Cahnge PQ27 SB000000AJ00(S TR AO4712 1N SO8) to SB0000004T80(S TR FDS6670AS_NL 1N SO8)	20080506	PVT
14	1.1V circuit change	BOM modify	0.1	41	Cahnge PL8 SH000009180 (S COIL 1UH +-30% MSCDRI-104RD-1R0N 11A) to SH000009180 (S COIL 1UH +-30% MSCDRI-104RD-1R0N 11A)	20080506	PVT
15	1.2V circuit change	For 0 degree not boot issue	0.1	40	Add PR185 SD013100180 (S RES 1/10W 1K +-5% 0603)	20080512	PVT
16							
17							
18							
19							
20							
21							
22							
23							

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NO	DATE	PAGE	MODIFICATION LIST	NO	DATE	PAGE	MODIFICATION LIST
3/15		P.06	Modify CPU DTS function Add R562,R565 Pop R344,R348,C410,Q32,Q33 Un-pop R560,R561,R563,R564 Change R345,R346 to 2.2K_0402	5/6			Update PW circuit
						P.06	Un-pop R344,R348,C410,Q32,Q33,R562,R565,R335 Remove R560,R563
		P.11	Change R55 to 140_0402_1% Un-pop Q2,R86,Q49,R411 Pop R85,R553			P.14	Change U15 clockgen to Silego ()
						P.24	Un-pop U39,C670 Change R532 to L79 (SM010005480)
		P.12	Change C95,C139,C129,C44 to 22u_0805 Pop L1,L2			P.35	Add R569, C678
						P.28	Change U16 to version:D1 (SA00001J550)
		P.16	Change R66 to 140_0402_1%			P.06	Add R570
		P.19	Change R550 to 4.7K_0402			P.22	Change JSATA1 footprint
		P.21	Change R87 to 2.2K_0402	5/6		P.12	Change L3 to R571, 0_0805
		P.26	Add R566	5/12			Update PW circuit
		P.32	Change R459,R460,R457,R458 to 1K_0402_1%			P.09	Add C679, C680
		P.34	Change R242 to 10K_0402	5/13		P.14	Add D39 for ESD
3/18		P.28	Pop R559			P.35	Add C681,C682,C683,C684,C685,C686 for EMI
		P.12	Change C15,C16,C17,C18 to 22u_0805			P.35	H4 become NPTH
		P.18	Pop R558			P.09	Udate PW circuit Add C687
3/19			Upgrade PW circuit	5/13		P.33	JHP1,JLINE1,JMIC1-->pin7,8 connect to AGND for ESD
		P.07	Change C195,C167 to 0402 package				
3/21		P.14	Change U15 to SA000023H10	6/02		P.22	Reserve C688,C689
							Update PW circuit
		P.11	Change C29 to 22u_0805	6/10		P.23	Add C690 for EMI
3/24		P.18	Change BT USB from port6 to port9.			P.24	Change C653~C656 to 100p for EMI
						P.35	Change C681 to 330p for EMI
		P.15	Add R567,R568,C677 Remove C357				Pop C683 for EMI
3/25		P.27	Pop L29,L30 Un-pop R139,R136,R143,R146			P.19	Change R550 to 10K
						P.12	Un-pop L1,L2
						P.28	Change U16 to version C0 (SA00001J540) Pop R226
		P.24	Change R542 to Bead (SM010005480)				Change R512 to 18K
3/26			Update some notice			P.29	Del U19 Pop U18 (128K--SA00002C100)
							Pop SB SPI ROM (R547,C675,R549,R548,R550,U40)
				7/1		P.19	Change L79 to 0_0805_5% Resistance
						P.24	
						P.31	Un-pop SW9

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